# Critical Dimension and Overlay Metrology Program

The principal productivity driver for the semiconductor manufacturing industry has been the ability to shrink linear dimensions. A key element of lithography is the ability to create reproducible undistorted images, both for masks and the images projected by these masks onto semiconductor structures. Lithography as a whole, fabricating the masks, printing and developing the images, and measuring the results, currently constitutes ≈35 % of wafer processing costs. The overall task of the Critical Dimension and Overlay Program is to assist the industry in providing the necessary metrology support for current and future generations of lithography technology. These goals include advances in modeling, the provision of next generation critical dimension and overlay artifacts, development of advanced critical dimension and overlay techniques, and comparisons of different critical dimension and overlay measurement techniques.

Currently, resolution improvements have outpaced overlay and critical dimension measurement improvements. To maintain cost effectiveness significant advances must be made.

# Wafer-Level and Mask Critical Dimension Metrology

This project is the single largest project at NIST supporting the semiconductor industry. It involves metrology and artifact development across a broad range of techniques. For this reason the project is presented in a number of sub-sections, each focusing on a single technology. These are:

- Scanning Electron-Based Dimensional Metrology
- Scanning Probe Microscope-Based Dimensional Metrology
- Small Angle X-Ray Scattering-Based Dimensional Metrology
- Electrical-Based Dimensional Metrology and Critical Dimension Reference Material Development
- Optical-Based Photomask Dimensional Metrology
- Model-Based Linewidth Metrology
- Atom-Based Dimensional Metrology

# Scanning Electron-Based Dimensional Metrology

## Goals

Provide the microelectronics industry with highly accurate SEM measurement and modeling methods for shape-sensitive measurements and relevant calibration standards with nanometer-level resolution.

Carry out SEM metrology instrumentation development, including improvements in electron gun, detection, sample stage and vacuum system.

Conduct research and development of new metrology techniques using digital imaging and networked measurement tools solutions to key metrology issues confronting the semiconductor lithography industry.

## Customer Needs

The scanning electron microscope is used extensively in many types of industry, including the more than $200 billion semiconductor industry in the manufacture and quality control of semiconductor devices. The industry needs SEM standard artifacts, specifically those related to instrument magnification calibration, performance and the measurement of linewidth. This entails a multidimensional program including: detailed research of the signal generation in the SEM, electron beam-sample interaction modeling, developing NIST metrology instruments for the certification of standards, and developing the necessary artifacts and calibration procedures. The manufacturing of present-day integrated circuits requires that certain measurements be made of structures with dimensions of 100 nm or less with a high degree of precision. The accuracy of these measurements is also important, but more so in the development and pilot lines. The measurements of the minimum feature size known as critical dimension (CD) are made to ensure proper device operation. The U.S. industry needs high-precision, accurate, shape-sensitive dimension measurement methods and relevant calibration standards. The SEM Metrology Project supports all aspects of this need since scanning electron microscopy is key microscopic technique used for this sub-100 nm metrology.

## Technical Strategy

The Scanning Electron Microscope Metrology Project a multidimensional project. It is being executed through several thrusts fully supported by the semiconductor industry.

**1. SEM Magnification Calibration Artifacts:** Essential to SEM dimensional metrology is the calibration of the magnification of the instrument. Standard Reference Material (SRM) 2120 is an SEM magnification standard that will function at the low beam voltages used in the semiconductor industry and high beam voltages used in other forms of microscopy (Fig. 1). Conventional optical lithography provides a chance for large amount of good quality samples produced inexpensively. Because of the improvements of this technology, it is now possible to produce the finest lines with close to 100 nm width and with 200 nm pitch values. The largest pitch is 1500 μm. In order to make this artifact available (while the final certification details are being completed) the artifact will be released as Reference Material (RM) 8120.

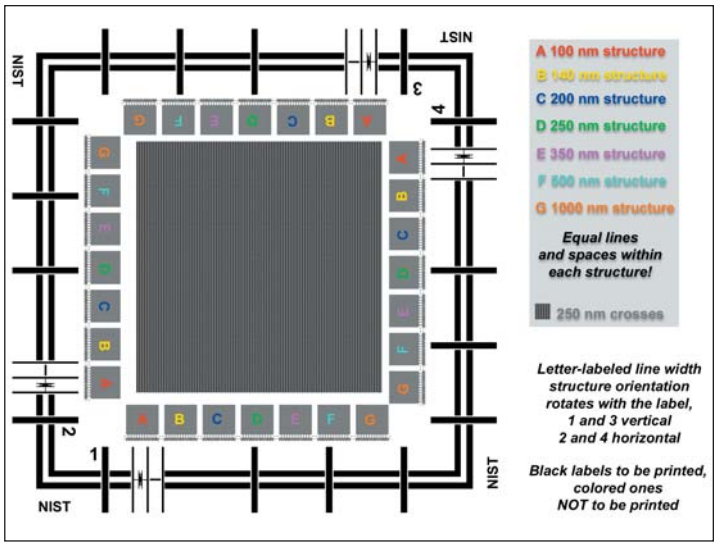


*Figure 1. The final design of the SRM 2120 magnification calibration standard reference material.*

**Technical Contacts:**
A. E. Vladar
J. S. Villarrubia
M. T. Postek

***"Scanning Electron Microscopy (SEM) – continues to provide at-line and inline imaging … and CD measurements. Improvements are needed … at or beyond the 65 nm generation … Determination of the real 3-D shape…will require continuing advances in existing microscopy …"***

*International Technology Roadmap for Semiconductors, 2003*

**DELIVERABLES:**

- Development of a new metrology SEM based on a variable pressure instrument. This instrument will be able to work with full size wafers and photomask.

- Preparation of an assessment of the error budget for the fully functional metrology system. Preparation of customized recipes for various versions of magnification calibration samples.

- Upon availability of suitable quality samples, quality assessment and delivery of a batch of RM 8120.

- Upon availability of suitable quality samples, completion calibration and delivery of a batch of SRM 2120 samples. 4Q 2005

**2. SEM Performance Measurement Artifacts**: This effort included the development of the Reference Material 8091 and evaluation procedures suitable for correctly measuring image sharpness of scanning electron microscopes, especially of those that are used in the semiconductor industry. The resolution performance characteristics of the SEM are particularly important to precise and accurate measurements needed for semiconductor processing. New methods and suitable samples are being sought to further improve this type of metrology. Several samples have been purchased by leading semiconductor manufacturing companies and these measurement artifacts are used in the benchmarking efforts of International SEMATECH. The existence of these samples fosters better understanding, objective measurement and enforcement of SEM spatial resolution performance.

**3. SEM Linewidth Measurement Artifacts:** Artifacts that are characterized and calibrated to the required small levels of uncertainty were and are in the focal point of the IC industry's dimensional metrology needs. Therefore, at NIST, it has been a longer-term goal to develop and deliver appropriate samples. For a long time the possibilities were limited by the lack of various technologies available, especially the lack of accurate modeling methods. NIST, through several years of systematic efforts, developed Monte Carlo simulation-based modeling methods that can deliver excellent results. These new methods can deduce the shape of integrated circuit structures from top–down view images through modeling and library–based measurement techniques with a few nm of accuracy. NIST in several publications demonstrated the possibilities and described power of this measuring approach. Based on the newest results, now it is becoming possible to start to develop the long–awaited relevant line width standard for the semiconductor industry. Reference Material 8120 line width samples will be a relevant sample on a 200-mm and 300-mm Si wafer with polySi features with sizes from 1 mm to down to 70 nm. Standard Reference Material 2120 is going to be the calibrated, traceable version for line width measurements. This work is being carried out in cooperation with SEMATECH.

**DELIVERABLES:**

- Design and preparation of line width metrology artifact suitable for calibration on NIST and external measuring systems for certification of wafer format line width samples.

- Completion of preliminary measurements on samples made by SEMATECH with the new "NISTMAG" metrology mask. 4Q 2005

## Accomplishments

■ **SEM Magnification Calibration Artifacts** – Samples for Reference Material 8090 have been made in the past once successfully, but later several attempts with e-beam lithography yielded no further useful samples. We now have a new, final mask designed and fabricated at International SEMATECH to get samples made by 193 nm UV light lithography. The use of this conventional lithography and a somewhat modified design provides a chance for large amount of good quality samples produced inexpensively. Because of this technology, it is now possible to produce the finest lines with close to 100 nm width and with 200 nm pitch values. The largest pitch is 1500 μm. There are a large number of 250 nm wide crosses for distortion and other measurements. Scatterometry patterns with varying pitches will also be available. The features on the conductive Si wafer will be formed from polySi material. These samples will give suitable contrast in any SEM to allow the user to set the magnification of the instrument from the smallest to the highest magnifications. The first wafers containing the final design were fabricated by International SEMATECH and found to be useful. The fabrication of the first large batch of samples will be finished in the summer of 2005. With the arrival of the new metrology SEM these will be calibrated.

■ **SEM Performance Measurements** – After comprehensive studies and experiments a plasma-etching Si called "grass" was chosen for Reference Material 8091 (Fig. 2). This sample has 5 nm to 25 nm size structures as is illustrated in the figure below. There have been 75 samples delivered

to the Office of Standard Reference Materials, NIST. A sharpness standard and evaluation procedure have been developed to monitor (or compare) SEM image quality. A NIST kurtosis method, Spectel Company's user-friendly analysis system called SEM Monitor, and University of Tennessee's SMART algorithm can be used with RM 8091. An effort is underway to produce more of these samples. These samples are now available to the public, and many of them are already in use.

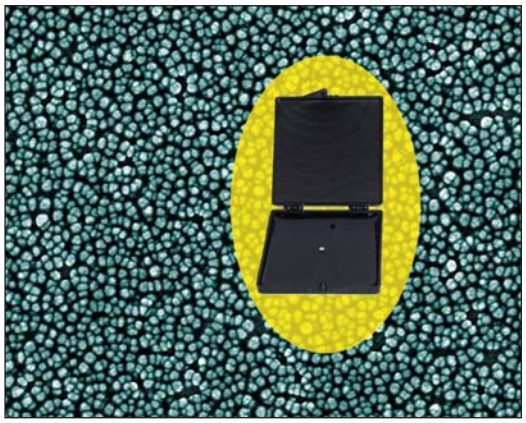

*Figure 2. The RM 9081 Sharpness Reference Material.*

■ **SEM Linewidth Measurement Artifacts** – For correct linewidth measurements accurate modeling methods are indispensable. The existing NIST methods have shown excellent results on polySi samples and they are under further development for higher accuracy. From a top-down view, using our high-accuracy modeling and fitting methods a cross section of the lines can be determined with few nm uncertainties and discrepancies. The match is so good that this method may be capable of eliminating the costly and destructive cross sectional SEM measurements. The candidate sample for linewidth artifact must be relevant to state-of-the-art IC technologies, should have chips on 200 mm and later 300 mm wafers with all process variation and include a meaningful focus-exposure matrix (FEM). The design and the fabrication of SEMATECH/NIST mask have been successfully completed. After CD-SEM measurements at SEMATECH, cross sectional measurements will be made at NIST. All these measurements will yield an excellent database for a decision on how to proceed with this wafer type linewidth reference sample. It is conceivable that by the end of the year 2005 the Reference Material 8120 line width samples will be available. This work is being carried out in close cooperation with SEMATECH.

■ **Development of High Accuracy Laser Interferometer Sample Stage for SEMs** – The development of a very fast, very accurate laser stage measurement system facilitates a new method to enhance the image and line scan resolution of SEMs. This method, allows for fast signal intensity and displacement measurements, and can report hundreds of thousands of measurement points in just a few seconds. It is possible then, to account for the stage position in almost real time with a resolution of 0.2 nm. The extent and direction of the stage motion reveal important characteristics of the stage vibration and drift, and helps minimize them. Figure 3 illustrates the short-term motion of the sample stage, the left side of the figure depicts the location of the stage and the right side is the density distribution of the location of the stage during 1 minute of dwell time. The field-of-views are 2 nm by 2 nm for each images. The high accuracy and speed also allow for a convenient and effective technique for diminishing these problems by correlating instantaneous position and imaging intensity. The new measurement technique developed recently gives a possibility for significantly improving SEM-based dimensional measurement quality. Important new discoveries made it possible to correctly understand the motion of the stage at the nm level, and the characterization of various settings and fine tuning of the sample stage, which is critical for high-resolution work.

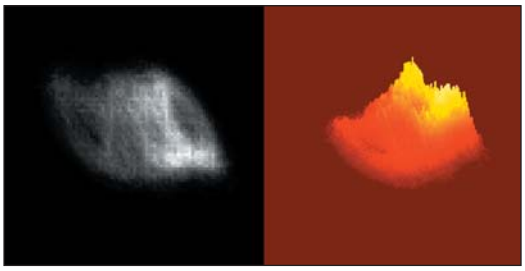

*Figure 3. Short-term motion of the SEM sample stage, the stage location (left) and its density distribution during a 1 minute of dwell time, 2 nm by 2 nm field-of-views.*

■ **Development of Line Edge Roughness Metrology for Integrated Circuit Technology** – The measurement of line-edge roughness (LER) has become an important topic in the metrology needed for the semiconductor industry. NIST has successfully developed various LER metrics and methods to make reliable and statically sound LER measurements. The findings have impact on the ITRS as they call for longer lengths for LER evaluation and on LER metrology in general

because the new methods offer significantly better metrology than what was available previously. The final report of a year-long study was delivered on time to SEMATECH.

■ **Development of Ultra-High Resolution Nano-tip Electron Gun for CD-SEMs** – The source diameter and the brightness of the electron beam are two of the major factors limiting the performance of CD-SEMs in the semiconductor production environment. Thus, alternative solutions to improve performance are being sought as the metrology for sub-100 nm lithography is being pushed to its limit. One possible alternative approach is the application of nano-tips as an electron source. Nano-tips, by comparison to conventional cold field, offer a substantial increase in brightness (10 x to 100 x) and a large reduction (5 x to 10 x) in source size. Figure 4 proves that the nano-tip electron gun can deliver 6 nm resolution images while the original gun's specification for the test microscope was only 15 nm. Therefore, in an optimized electron optical column, substitution of a CFE source by a nano-tip could be expected to produce:

- Higher beam currents into a spot of given size,
- Better signal-to-noise ratio and resolution, and
- Faster scan rate and better charge control.

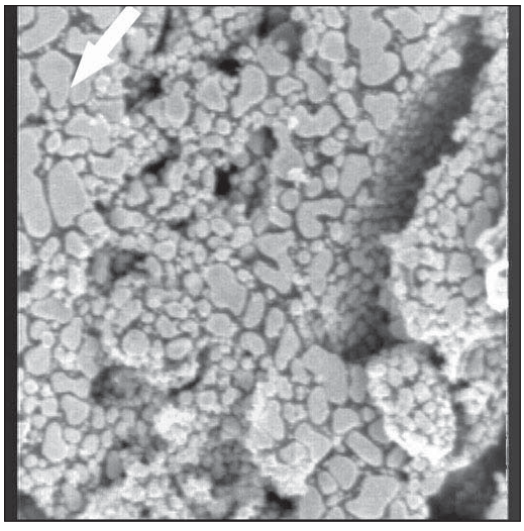

*Figure 4. Nano-tip electron gun image showing 6 nm resolution taken on a gold-on-carbon resolution sample at 900 V accelerating voltage. The SEM original specification resolution is 15 nm. The field-of-view is 1.75 μm.*

This work has proved that nano-tips indeed improve the resolution performance of SEMs and can be used for longer periods of time. Currently further experiments are conducted to assess the optimal setting of the electron gun and the electron optical column and life time and stability parameters of the nano-tips.

## Collaborations

International SEMATECH, Metrology Council.

International Technology Roadmap for Semiconductors; Microscopy and Metrology Sections.

## Recent Publications


Nano-tip Electron Gun for the Scanning Electron Microscope András E. Vladár, Zsolt Radi, Michael T. Postek and David C. Joy 2005 (in press).

A. E. Vladar, R. Silver, J. Potzick, J. S. Villarrubia and M.T. Postek 2004 Development of Photomask Artifacts and Metrology Methodology for the 65 nm Device Generation with Extensibility Beyond - SEMATECH Final Report

Line Edge Roughness Metrology for Integrated Circuit Technology, Vladár A. E., Villarrubia J. S., Dixson R., Vorburger T., Orji N. G., Bunday B. D., and Bishop M. Final Report to International SEMATECH (March 2004).

Laser Sample Stage-based Image Resolution Enhancement Method for SEMs, Vladár A. E., Jayewardene E. C., Damazo B. N., Keery W. J., and Postek M. T. SPIE 2004 5375-181.

New Method for the Measurement of SEM Stage Vibrations, Damazo, B. N., Jayewardene E. C., Vladár A. E., Keery, W. J., and Postek M. T. 2004. SPIE 2004.

A New Way of Handling Dimensional Measurement Results for Integrated Circuit Technology, András E. Vladár, John S. Villarrubia and Michael T. Postek, Proc. SPIE 5038, 2003, pp. 508-517.

Test of CD-SEM Shape-Sensitive Linewidth Measurement, J. S. Villarrubia, A. E. Vladár, and M. T. Postek, Final Report to International SEMATECH (2003).

Exploring and Extending the Limits of SEMs' Resolution, A. E. Vladár, J. S. Villarrubia, and M. T. Postek, Final Report to International SEMATECH (November 2003).

New Application of High Pressure/Environmental Microscopy to Semiconductor Inspection and Metrology, Postek, M. T. and Vladár, A. E. SCANNING (2003).

Is Low Accelerating Voltage Always Required for Semiconductor Inspection and Metrology? Postek, M. T. and Vladár, A. E. Microscopy Microanalysis IX pp. 978-979 (2003).

Information Transfer Capability and Signal Processing Performance of Modern Scanning Electron Microscopes, Radi. Z, Vladár, A. and Postek, M. T. Microscopes and Microanalysis IX pp. 762-763 (2003).

Photomask Dimensional Metrology in the SEM Part I: Has Anything Really Changed? Postek, M. T., Vladár, A. E., Bennett, M. H. Journal of Microlith., Microfab and Microsystems (2003).

Photomask Dimensional Metrology in the SEM Part II: High Pressure/Environmental SEM, Postek, M. T., Vladár, A. E., Bennett, M. H., Rice, T., and Knowles, R. Journal of Microlith., Microfab and Microsystems (2003).

Application of High Pressure/Environmental Scanning Electron Microscopy to Photomask Dimensional Metrology, Postek, M. T. and Vladár, A. E. Characterization and Metrology for ULSI Technology (D. Seiler et al. eds) AIP Press, New York (2003).

# Scanning Probe Microscope-Based Dimensional Metrology

## Goals

Improve the measurement uncertainty of critical-dimension measurements in the semiconductor industry through improvements in SPM-based measurements. *The International Technology Roadmap for Semiconductors (ITRS)* identifies dimensional metrology as a key enabling technology for the development of next-generation integrated circuits. For example, according to the 2003 edition, the goal in 2004 for critical dimension (CD) measurement precision for isolated lines was ± 0.8 nm; this demand tightens to ± 0.4 nm by 2009. The technical focus of this project, development and implementation of scanned probe microscope instrumentation, is driven by the anticipated industry needs for reduced measurement uncertainty, particularly for existing tools such as the SEM.

## Customer Needs

The SEM is the current tool of choice for inspection and metrology of sub-micrometer features in the semiconductor industry. SPMs possess unique capabilities, which may significantly enhance the performance of SEMs for in-line critical dimension (CD) measurements, and are also emerging as CD measurement tools in their own right. A creative strategy, which successfully harnesses the strong points of both techniques in order to reduce the measurement uncertainty of sub-micrometer features, will help NIST meet the expectations of the semiconductor industry expressed in the current *ITRS*. As is the case with SEMs, the magnification or scale of an SPM must be calibrated in order to perform accurate measurements. Although many SPMs are commercially available, appropriate calibration standards have lagged. In particular, traceable pitch/height standards with sub-micrometer pitch values are not yet available.

## Technical Strategy

SPM development is proceeding along two parallel directions: The first direction addresses dimensional metrology of SPM specifically through two in-house research instruments, a calibrated atomic force microscope for measurement of pitch and step height and a critical dimension atomic force microscope (CD-AFM) for measurement of line width. The C-AFM has metrology traceable to the wavelength of light for all three axes of motion and has provided calibrated pitch and height measurements for nanoscale applications. Pitch, ranging up to 20 μm has been measured with standard uncertainties ($u_c$) as low as ≈0.5 nm at submicrometer scales and relative standard uncertainties of ≈0.1 % at the largest scales. Step height, ranging from a few nanometers up to several hundred nanometers, can be measured with $u_c$ on the order of 0.5 % at the largest scales. Calibration procedures have been developed for linewidth measurements using the CD-AFM acquired in FY04. As part of the project, we have also begun to pursue research in the measurement and standardization of line edge roughness.

**DELIVERABLES:** Presented paper at 2005 ULSI conference on a two sample inter method comparison of image stitching linewidth metrology using carbon nanotube tips with CD-AFM measurements. 2Q 2005

**DELIVERABLES:** Completed analysis of CD-AFM data to complete the single crystal critical dimension reference material (SCCDRM) project with EEEL and presented paper on methodology at SPIE Microlithography meeting. 2Q 2005

**DELIVERABLES:** Perform C-AFM measurements to participate in an international Supplementary Key Comparison in Nanometrology on two dimensional pitch measurements. 4Q 2005

**DELIVERABLES:** Publish Final Report to SEMATECH on the development of a CD-AFM Reference Measurement System (RMS) – the work performed during Ronald Dixson's tenure as a NIST Guest Scientist at SEMATECH. 3Q 2005

**DELIVERABLES:** Perform SXM measurements of pitch and height on OMAG3L wafer to support the SRM2089 release in FY06. 4Q 2005

The second direction addresses increasingly overlapping demands for dimensional control during fabrication and subsequent calibration of nanometer scale features. For this purpose we employ an SPM-based lithography technique, pioneered at NIST, to produce grating structures with linewidths of 20 nm or below. Latent oxide patterns function as masks for anisotropic wet or dry etching. We are also developing an instrument that integrates both SPM and probe station measurement capabilities whereby we are able to compare SPM-based electrical (capacitance and

**Technical Contacts:**
T. V. Vorburger
J. A. Dagata
R. Dixson
M. T. Postek

surface potential) and topographical measurements of active device structures simultaneous with traditional current-voltage (IV) characteristics measured with a probe station. This allows us to examine local nanoscale variations at exposed and buried interfaces of critical dimensioned features in order to identify processing induced variations which contribute to linewidth uncertainty in dimensional and electrical test structures.

**DELIVERABLES:** Develop a predictive model for SPM oxidation kinetics for optimized linewidth control of latent oxide features. This model will include the influence of electronic and ionic transport on the intrinsic thickness growth and lateral spreading due to space charge.

**DELIVERABLES:** Investigate anomalous features on the growth and breakdown of Group 4 metal films (Ti, Zr, Hf) and their nitrides during local oxidation.

## Accomplishments

■ Ronald Dixson completed a three year tenure as the first NIST Guest Scientist at International SEMATECH, and returned to NIST in 4QFY04. During his tenure, he developed the CD-AFM reference measurement system (RMS) at SEMATECH for traceable measurements of pitch, height, and width. Measurements were also performed to support the EEEL linewidth standards project which is discussed below. In 3QFY05, George Orji became the second NIST Guest Scientist and will build upon the partnership that NIST and SEMATECH have established.

■ We are collaborating with other NIST divisions and external partners such as SEMATECH to develop linewidth standards. A major component of this effort has been the single crystal critical dimension reference materials (SCCDRM) project initiated by NIST researchers in EEEL (Cresswell and Allen). The 2004 release of SCCDRM samples to the SEMATECH Member Companies was recently completed, and CD-AFM dimensional metrology played a central role. The measurements on the SCCDRM samples were performed by NIST scientist Ronald Dixson during his tenure as a Guest Scientist at SEMATECH. A current generation CD-AFM (a Veeco Dimension X3D) which had been implemented as an RMS was used for the SCCDRM measurements. Prior to the measurements, the X3D was characterized and calibrated, and implemented as a reference measurement system (RMS) for traceable measurements of pitch, height, and width. High resolution transmission electron microscopy (HRTEM) was used as an indirect method of tip width calibration for the SCCDRM samples. The AFM and HRTEM results that were used for the tip calibration are shown in Fig. 1. Features on the distributed samples ranged in width from approximately 50 nm to 250 nm with expanded uncertainties of about 2 nm ($k = 2$) on most features. As a result of this project, CD-AFM linewidth measurements can now be performed with a 1 nm ($k = 1$) standard uncertainty.

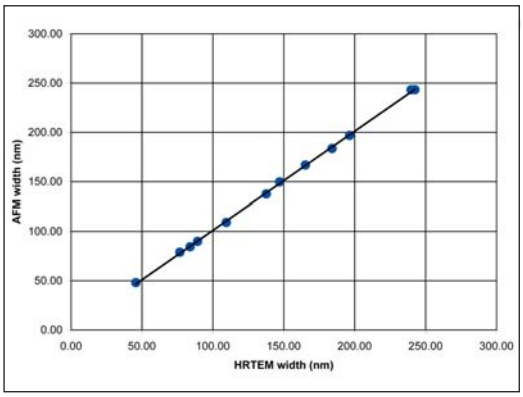


*Figure 1. Regression of CD-AFM width values on HRTEM values. The observed slope is consistent with unity – indicating that the two methods have consistent scale calibration. The average offset between the results was used to correct the tip width calibration.*

■ We are participating in a series of International Supplementary Comparisons in nanometrology coordinated by the CIPM (Comité International des Poids et Mesures) CCL (Coordinating Committee for Length). Successful participation in these Comparisons will facilitate international recognition of NIST-traceable measurements of dimensional quantities important to the semiconductor industry. The results from NIST and other national measurement institutes (NMIs) for step height and grating pitch have now been published under the Mutual Recognition Arrangement (MRA) through which the NMIs recognize each other's measurement capability, thus helping to eliminate technical barriers to trade. A comparison of 2-D pitch is presently underway, with NIST participation scheduled for Sept. 05, and a linewidth comparison is in the planning stage.

■ Another effort involves the study of single atomic Si steps as fundamental height standards in the sub-nanometer regime. During 2004 we developed a draft standard for AFM z-calibration using the single atom steps for the ASTM Sub-

committee E42.14 on STM/AFM. It is currently undergoing review.

■ We are developing a technique for AFM linewidth metrology based on image stitching. This involves the acquisition of paired images using a carbon nanotube probe. The nanotube tip enables data acquisition at high resolution on one side of the line in each image, and the specimen is rotated 180 degrees between the two measurements. Stitching these two images into a composite offers the potential of accurate linewidth metrology. We have completed two generations of an experiment in which the stitching result is compared with CD-AFM. The composite image used in one of our published comparisons between image stitching and CD-AFM is shown in Fig. 2. Currently, we are assessing the uncertainties and continuing to refine this approach.

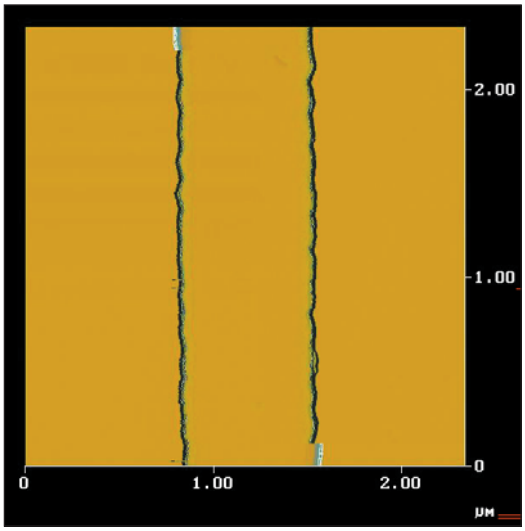


*Figure 2. Stitched composite slope image from two images of a linewidth sample taken with a carbon nanotube tip. Measurements performed by J. Fu; sample developed by M. Cresswell and R. Allen; probe developed by C. Nguyen of ELORET/NASA Ames.*

■ The commonly used AFM-based method of linewidth metrology in industry is CD-AFM. This type of instrument is more sophisticated than conventional AFM and used a flared shape probe and two-dimensional feedback to image the sidewalls of near-vertical structures. As a consequence of Ronald Dixson's tenure as a NIST Guest Scientist at SEMATECH, we were able to acquire an older generation CD-AFM when SEMATECH purchased a newer one. An image of a SCCDRM specimen taken with this instrument is shown in Fig. 3. We have developed pitch, height, and width measurement uncertainty budgets for this instrument. As a consequence of the completion of the SCCDRM project, we can now calibrate CD-AFM tip width with an uncertainty of 1 nm.

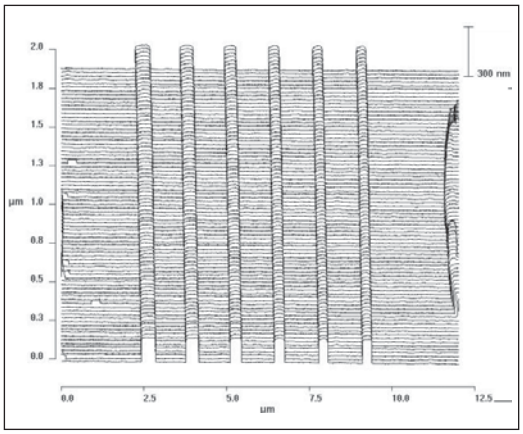


*Figure 3. CD-AFM image of a NIST45 SCCDRM specimen which can be used for tip width calibration. Measurements performed by R. Dixson, sample developed by M. Cresswell and R. Allen.*

■ We are also working on development of AFM-based techniques for traceable measurement of physical standards for line edge roughness (LER), a potential showstopper in the *ITRS.*

■ In the integrated SPM probe-station thrust, we have completed systematic low-noise (sub-pA) measurements of current flow during SPM oxidation of silicon substrates. Two methods of data acquisition were employed, measurements made directly as a function of voltage, humidity, and exposure time during contact-mode oxidation and those made during a (so-called) force vs. distance curve in which a biased SPM probe tip approaches, contacts, and retracts from a substrate (see Fig. 4, pg. 32). In the latter, electrostatic bending of the SPM cantilever can be easily modeled and the bending capacitance calculated. Electronic and ionic currents have been identified and their consequences for oxide growth and space-charge buildup during lithography have been determined. The role of the water meniscus as a conduit under noncontact oxidation has been clarified.

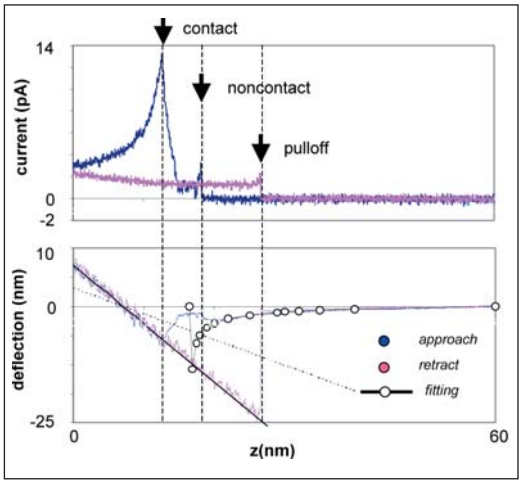


*Figure 4. Simultaneous SPM current vs. distance (a) and force vs. distance (b) curves for an 18.5-V biased silicon probe tip approaching, contacting, and retracting from a silicon substrate at 65 % RH. A small 2-pA current flows through the nanometer-scale water meniscus that forms at the junction. A much larger 12-pA current flows when the tip makes hard contact with the substrate.*

■ As part of the integrated SPM probe-station thrust, we have also begun studying anomalous oxide growth kinetics in the Group 4 metal films (Ti, Zr, Hf) and their nitrides. In addition to insight into potential defect behavior in alternative dielectrics, SPM kinetic studies of these films reveal new insight into ionic and electronic transport in local oxides that are quite different than in other systems (see Fig. 5).

## Collaborations

Departments of Mechanical Engineering and Chemistry, University of North Carolina, Charlotte

IBM Almaden Research Center, San Jose, CA

School of Mechatronic Engineering, Harbin Institute of Technology, Harbin, China.

ELORET Corp./ NASA Ames Research Center, Moffett Field CA.

Departments of Physics and Engineering, University of Akron, Akron OH

National Institute of Advanced Industrial Science and Technology, Tsukuba Japan

National Microelectronics Center of Spain, Barcelona Spain

Center for Measurement Standards, Industrial Technology Research Institute, Hsinchu Taiwan

Department of Physics, National Tsing-hua University, Hsinchu, Taiwan

SEMATECH, Austin TX

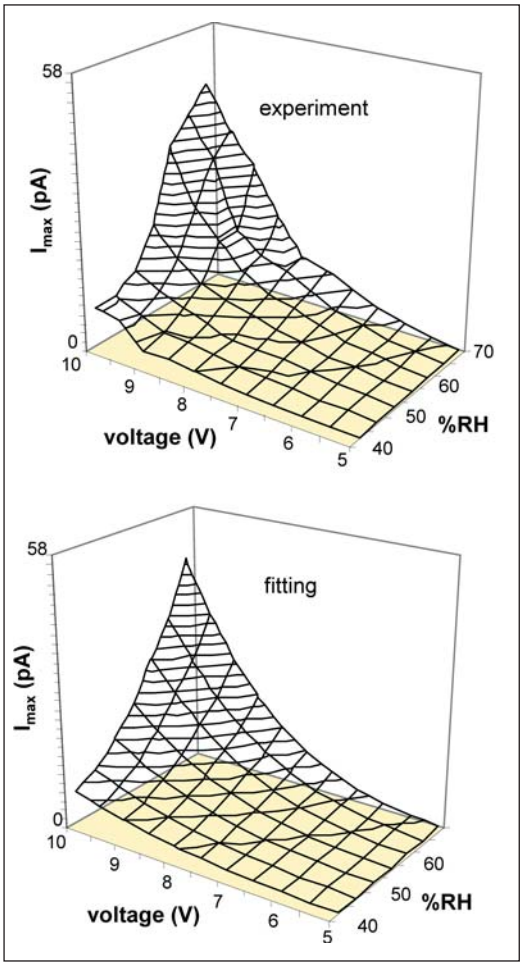


*Figure 5. Experiment (a) and modeling (b) of the maximum current achieved during SPM local oxidation as a function of voltage and humidity. The SPM tip used in these experiments was coated with a PtRh metal film and the substrate was hydrogen-passivated n-type Si(100).*

## Recent Publications

J. Fu, R. Dixson, N. Orji, T. Vorburger, C. Nguyen, "Linewidth Measurement from a Stitched AFM Image," to be published in *Characterization and Metrology for ULSI Technology: 2005 International Conference,* (2005).

R. Dixson, J. Fu, N.G. Orji, W. Guthrie, R. Allen, M. Cresswell, "CD-AFM Reference Metrology at NIST and SEMATECH," to be published in Proc. SPIE **5752**, (2005).

M. Cresswell, R. Dixson, W. Guthrie, R. Allen, C. Murabito, B. Park, J. Martinez, A. Hunt, "Critical Dimension Reference Features with Sub-Five Nanometer Uncertainty," to be published in Proc. SPIE **5752**, (2005).

N.G. Orji, M.I. Sanchez, J. Raja, and T. Vorburger, "AFM Characterization of Semiconductor Line Edge Roughness," in *Applied Scanning Probe Methods,* edited by B. Bhushan, H. Fuchs, and S. Hasaka (Springer Verlag, Berlin, 2004) p. 273.

B.D. Bunday, M. Bishop, D. McCormack, J.S. Villarrubia, A.E. Vladar, R. Dixson, T. Vorburger, N.G. Orji, J.A. Allgair, "Determination of Optimal Parameters for CD-SEM Measurement of Line Edge Roughness, Proc. SPIE **5375**, (2004).

N. Sullivan, R. Dixson, B. Bunday, M. Mastovich, P. Knutrud, P. Fabre, and R. Brandom, "Electron Beam Metrology of 193 nm Resists at Ultra Low Voltage," Proc. SPIE Proc. **5038,** 483 (2003).

J. Fu, H. Zhou, J. Kramar, and R. Silver, "Dependence of Morphology on Miscut Angle for Si(111) etched in NH4F," Appl. Phys. Lett. **18**, 3014 (2003).

R. Dixson and A. Guerry, "Reference Metrology Using a Next generation CD-AFM," Proc. SPIE **5375**, 633 (2004).

L. Koenders, R. Bergmans, J. Garnaes, J. Haycocks, N. Korolev, T. Kurosawa, F. Meli, B.C. Park, G.S. Peng, G.B. Picotto, E. Prieto, S. Gao, B. Smereczynka, T. Vorburger, and G. Wilkening, "Comparison on Nanometrology: Nano 2 – Step Height, Metrologia **40**, (Technical Supplement 2003) 04001.

R.A. Allen, M.W. Cresswell, C.E. Murabito, R.G. Dixson, and E.H. Bogardus, "Critical Dimension Calibration Standards for ULSI Metrology" C*haracterization and Metrology for ULSI Technology: 2003 International Conference, CP683* (Amer. Inst. Phys., Melville, NY, 2003) p. 421.

X. Zhao, J. Fu, W. Chu, C. Nguyen, and T. Vorburger, "An Image Stitching Method to Eliminate the Distortion of the Sidewall in Linewidth Measurement, Proc. SPIE **5375,** 363 (2004).

Dagata, J. A.; Perez-Murano, F; Martin, C.; Kuramochi, H.; and Yokoyama, H.; *Current, charge, and capacitance during scanning probe oxidation,* Parts I&II, J. Appl. Phys. (in press).

Jun, J; Chien, F.S.; Hsieh, W.F.; Gwo, S; Silver, R. M.; Vladar, A. E.; Dagata, J.A., *Calibration of a Prototype Silicon Pitch Standard by Scanning Probe Oxidation and Anisotropic Etching*, J. Res. NIST (in preparation).

Schmitz, T. L.; Dagata, J. A.; Dutterer, B.; and W. G. Sawyer, *Nanolithography and Microfluidics: A Manufacturing Perspective*, J. Manufacturing Processes, in press.

Farkas, N.; Zhang, G.; Evans, E. A.; Ramsier, R. D.; Dagata, J. A., *Local oxidation of metal and metal-nitride films*, J. Vac. Sci. Technol. A, (Jul/Aug) 2004.

Farkas, N.; Zhang, G.; Evans, E. A.; Ramsier, R. D.; Dagata, J. A., *The role of subsurface oxygen in the local oxidation of zirconium and zirconium nitride thin films*, Thin Solid Films **447-448** 468 (2004).

Kuramochi, H.; Perez-Murano, F; Dagata, J. A.; and Yokoyama, H.; *Faradaic current detection during anodic oxidation of the H-passivated p-Si(001) surface with controlled relative humidity*, Nanotechnology **15** 297 (2004).

# Small Angle X-Ray Scattering-Based Dimensional Metrology

**Technical Contacts:**
Ronald L. Jones
Eric K. Lin
Wen-li Wu

## Goals

To develop a small angle X-ray scattering (SAXS)-based methodology to quickly, quantitatively, and non-destructively measure critical dimensions (CD) and feature shape with sub-nanometer resolution on production scale test samples. Quantities of interest include critical dimension, sidewall angle, and statistical deviations across large areas. Of particular focus is delivering a technique capable of routine measurement of pattern shape, including critical dimension, sidewall angle, line width fluctuations, and line edge roughness, in dense high aspect ratio patterns possessing sub-50 nm critical dimensions. In addition to addressing the metrological needs of future technology nodes, the sub-Angstrom wavelengths utilized by SAXS based measurements well complement current metrological tools based on optical scatterometry, SEM, and AFM.

## Customer Needs

The drive to reduce feature sizes to sub-50 nm technology nodes outlined by the SEMATECH Roadmap continues to challenge metrology techniques for pattern characterization. As pattern sizes decrease, existing techniques such as CD-SEM face significant technical hurdles in imaging quantities such as Line Edge Roughness (LER). Emerging metrologies based on techniques such as atomic force microscopy are still being evaluated, providing a lack of clear definition in suitable metrology for standardized measurements of both organic and inorganic structures. To address these issues, NIST is evaluating the potential application of small angle x-ray scattering as a metrology tool for both process development and the production of standards for industrially practiced metrologies such as CD-SEM.

## Technical Strategy

1. Exposure systems capable of sub-50 nm patterning are expected by 2009, requiring control of CD on the level of nanometers and in some cases sub-nanometer precision. These requirements will challenge traditional methods including CD-SEM and optical scatterometry. We are developing a transmission scattering based method capable of angstrom level precision in critical dimension evaluation over large (50 μm x 50 μm) arrays of periodic structures (see Fig. 1). In contrast to optical scatterometry, SAXS is performed in transmission (see Fig. 1) using a sub-Angstrom wavelength. The high energy of the X-ray allows the beam to pass through a production quality silicon wafer, and is therefore amenable to process line characterization. As with optical scatterometry, the measurements are performed in ambient conditions, minimizing time required for sample preparation. The current capabilities of commercially available X-ray sources and detectors suggest that the technique is portable to a laboratory scale device capable of high precision measurements. NIST has designed and expects to implement the world's first laboratory scale CD-SAXS device.

**DELIVERABLES:** Install and evaluate laboratory scale CD-SAXS instrument 4Q 2005

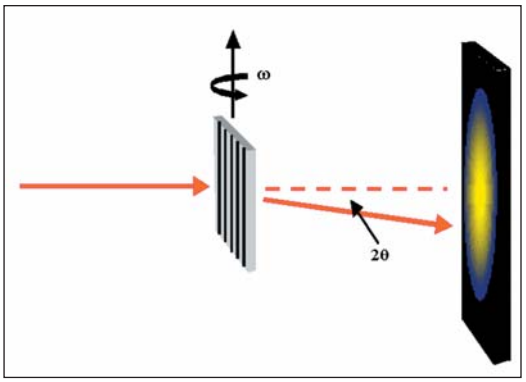


*Figure 1. Schematic of the SAXS transmission geometry. Shown is the x-ray beam (solid line) as it passes through the patterned sample and scattered at an angle 2θ. For a precisely aligned sample with known composition, a 3-d lineshape is obtained in one transmission measurement. Unknown samples can also be characterized through measurements at a variety of sample angles.*

2. Characterization of pattern quality includes shape factors such as the sidewall angle and curvature. Using the above protocol for scattering, measurements taken at a series of angles of incidence allows the reconstruction of the line shape. We have performed tests using multiple angles on a test grating and determined an ability to measure sidewall angle to within 1 degree. Ongoing analysis and technique refinement will provide

additional shape factors, allowing determination of more complex shape information such as sidewall curvature. In addition to a "high speed," model dependent characterization performed in a single measurement, a second method will be developed based on measurements at multiple sample orientations. This method provides a more precise picture of the entire pattern cross section analogous to cross sectional SEM in a non-destructive and model independent manner. In the current technology node, this measurement will be critical to the evaluation of optical scatterometry models for line shape, while providing a general capability to measure a pattern of arbitrary cross section in future technology nodes.

**DELIVERABLES:** Develop and publish methodology for sidewall angle measurements with CD-SAXS. 3Q 2004

3. Current LER and CD specification of LER in CD budgets requires high precision metrology for both quality control by vendors as well as quality assessment by customers. Metrologies such as CD-SEM, a top down technique, measure qualitatively different quantities compared to that of optical scatterometry and AFM. Our approach is to provide metrology of sidewall roughness, where sidewall roughness is defined by deviations from the average sidewall plane on length scales smaller than the CD. In cooperation with the Advanced Metrology Working Group at SEMATECH, NIST has designed a series of structures to model different types of roughness. CD-SAXS data from these structures will help further develop modeling protocols.

**DELIVERABLES:** Design, procure, and measure LER model structures with CD-SAXS. 4Q 2005

4. As circuit designs increase in complexity, next generation metrologies require capabilities to characterize patterns that deviate substantially from line/space patterns. As an example, a capability to precisely characterize dense arrays of high aspect ratio vias non-destructively is needed. The use of a 2-D collimated beam and a 2-D detector in the CD-SAXS technique provides a natural capability to characterize patterns such as vias, posts, and via pads. While the capability to observe such structures has previously been demonstrated, routine analysis of this class of structures has not been achieved. Using a series of patterns including vias of diameter less than 60 nm, we are developing specific experimental protocols, extending those developed for line/space patterns, to provide a data set capable of describing a precise pattern shape in 2-D arrays of patterns.

**DELIVERABLES**: Provide measurements and model describing the measurement of 2-D arrays of 60 nm via patterns. 4Q 2005

5. CD-SAXS measurements can be applied towards several other important problems for both semiconductor and next-generation nanofabrication technologies. CD-SAXS measurements are being evaluated as a potential measurement method capable of determining the densification of the sidewall of plasma etched, patterned nanoporous low-κ dielectric films. Electron microscopy has been used, but has been unable to measure the densification profile with sufficient resolution. In addition, CD-SAXS measurements can be used to evaluate the fidelity of pattern transfer with the nanoimprint lithography (NIL). In NIL, the pattern from a hard, master mold is transferred into an underlying organic material through mechanical pressure and elevated temperature or curing with ultraviolet light. CD-SAXS measurements of both the mold and the resulting pattern can be compared to evaluate the quality of the NIL structure.

**DELIVERABLES:** Determine feasibility of SAXS measurement methods for sidewall damage characterization in plasma etched patterned low-κ dielectric materials. 4Q 2005.

**DELIVERABLES:** Apply CD-SAXS measurements for the evaluation of the fidelity of pattern transfer in nanoimprint lithography and to measure the properties of nanoimprinted polymer nanostructures. 3Q 2005.

## Accomplishments

■ We have provided the first measurements of sidewall angle using small angle X-ray scattering (SAXS). Using a series of photoresist gratings produced at the IBM T. J. Watson Research Center (Q. Lin), CD-SAXS was performed using at the Advanced Photon Source (Argonne National Laboratory) to measure photoresist patterns with well-defined sidewall angles. The protocol involves measurements of the sample over 20 degrees of incident angles, and reconstructing the Fourier representation of the pattern cross section. For a pattern with trapezoidal cross section, ridges of intensity propagate at twice the sidewall angle (see Fig. 2). The existence of the ridges is a model independent check on the validity of the trapezoidal model, while different shapes, such as

a T-topped line, will produce different scattering patterns. The protocol is generalizable to other pattern shapes.

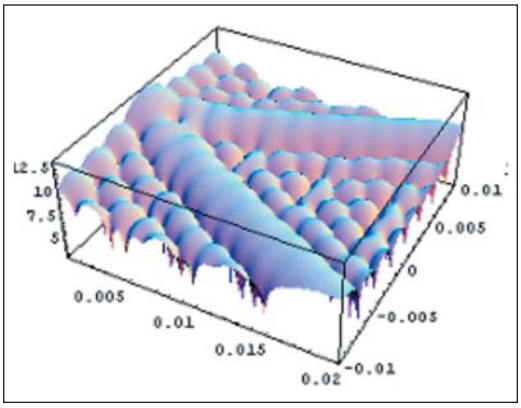


*Figure 2. Model of the expected scattering in the plane parallel to the line cross section. Calculation assumes a trapezoidal cross section. The sidewall angle is obtained by the half angle between the prominent ridges.*

■ Demonstrated a capability to measure correlated fluctuations in line edge position using CD-SAXS measurements of a series of line/space patterns in a "193 nm" photoresist produced at IBM T. J. Watson Research Center (A. Mahorawala) (see Fig. 3). These samples are believed to possess systematic, small shifts in the pattern. These shifts provide insight into measurements of line edge roughness (LER) where the roughness is highly correlated. The resulting data shows distinct streaks of intensity emanating from the diffraction peaks, particularly strong in the lower order peaks. These represent the first evidence of a capability of CD-SAXS to measure different types of defects related to the overall line edge roughness.

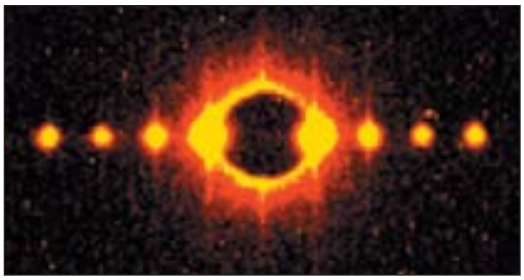

*Figure 3. Detector image of a 193 nm photoresist of an approximately 1:1 line/space pattern with a total repeat of 240 nm. In addition to the typical diffraction spots characterizing pitch and linewidth, streaks of intensity are observed emanating from the diffraction peaks. The streaks are a result of correlated roughness.*

■ Demonstrated a capability to measure a dense array of vias where the diameter of the vias were etched into a plastic substrate are less than 60 nm (see Fig. 4). Vias were etched into a produced into a plastic substrate at the IBM Almaden research center (M. Sanchez). The result demonstrates the capability of CD-SAXS to probe dense vias of sub-100 nm size. Ongoing work will attempt to provide a protocol for the evaluation of the full 3-D via shape as demonstrated for line/space patterns.

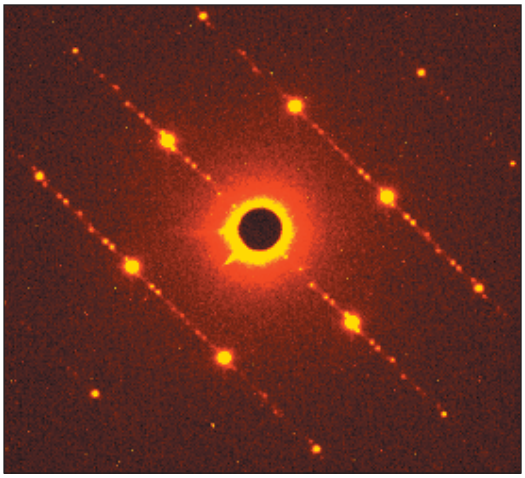

*Figure 4. CD-SAXS detector image resulting from a dense array of 60 nm vias. The array of diffraction patterns suggests an approximately hexagonal packing of the vias.*

■ Initial feasibility studies have demonstrated the potential of CD-SAXS to detect and to estimate the extent of sidewall damage of nanoporous low-κ materials patterned into line/space patterns. Previously, NIST had demonstrated that blanket low-κ films exposed to a plasma etch can have a skin layer with increased density and less hydrogen that may reflect the collapse of the pore structure. Since plasma etch effects can lead to an increase in k, it is important to measure the sidewall structure (porosity, electron density, etc.) of patterned low-κ films. To address this challenge, SEMATECH provided line gratings etched in a candidate low-κ material, then backfilled the trenches with the same candidate low-κ material. This backfilled sample simplifies modeling efforts and highlights the damaged regions to X-rays.

■ The real time shape evolution of nanoimprinted polymer patterns were measured as a function of annealing time and temperature using Critical Dimension Small Angle X-ray Scattering (CD-SAXS). Periodicity, linewidth, line height,

and sidewall angle were determined with nanometer resolution for parallel line/space patterns in poly(methyl methacrylate) (PMMA) both below and above the bulk glass transition temperature ($T_G$). Heating these patterns below $T_G$ does not produce significant thermal expansion, at least to within the resolution of the measurement. However, above $T_G$, the fast rate of pattern melting at early time transitions to a slowed rate in longer time regimes. The time dependent rate of pattern melting was consistent with a shape dependent thermal stability, where sharp corners possessing large Laplace pressures accelerate pattern dynamics at early times.

## Collaborations

SEMATECH, Ben Bunday, Pattern production and correlation to optical scatterometry (also through Advanced Metrology Advisory Group).

SEMATECH, Youfan Liu, Metrology of low-κ patterns using CD-SAXS.

Advanced Photon Source, Argonne National Laboratory, Diego M. Casa and John Quintana, Small Angle X-ray Scattering Instrumentation Development.

University of Michigan, Stella Pang, Ronald M. Reano, Nanoimprinted polymeric structures.

Intel Corporation, Kwang-Woo Choi, Bryan Rice, sub-50 nm structures.

Motorola, Doug Resnick. Characterization of sub-50 nm structures including dense arrays of posts.

IBM Almaden, Martha Sanchez, Characterization of sub-50 nm structures.

IBM Yorktown Heights, Arpan Mahorowala, Development of models for correlated line edge roughness scattering in line/space patterns.

IBM Yorktown Heights, Qinghuan Lin, Development of pattern shape and sidewall angle metrology.

## Recent Publications

R. L. Jones, E. K. Lin, Q. Lin, S. J. Weigand, D. T. Keane, J. P. Quintana, W. L. Wu, "Cross Section and Critical Dimension Metrology in Dense High Aspect Ratio Patterns with CD-SAXS," in Proceedings of the International Conference on Characterization and Metrology for ULSI Technology, March, 2005, Dallas, TX.

R. L. Jones, C. L. Soles, E. K. Lin, W. Hu, R. M. Reano, S. W. Pang, S. J. Weigand, D. T. Keane, J. P. Quintana, "Pattern Fidelity in Nanoimprinted Films using Dimension Small Angle Scattering," in Proceedings of the SPIE: Metrology, Inspection, and Process Control for Microlithography XVIII, March 2005, San Jose, CA.

R. L. Jones, T. Hu, C. L. Soles, E. K. Lin, R. M. Reano, S. W. Pang, D. M. Casa, "Real Time Shape Evolution of Nanoimprinted Polymer Structures during Thermal Annealing," Nano Lett., in press (2005).

T. Hu., R. L. Jones, E. K. Lin, W.-L. Wu, Q. Lin, D. Keane, S. Weigand, J. Quintana "Small angle X-ray scattering metrology of side wall angle and cross section in nanometer scale gratings," J. Appl. Phys. 96, 1983 (2004).

R. L. Jones, T. Hu, E. K. Lin, W. L. Wu, R. Kolb, D. M. Casa, P. J. Bolton, and G. G. Barclay, "Small angle x-ray scattering for sub-100 nm pattern characterization," Appl. Phys. Lett., 83, 4059 (2003).

W. L. Wu, E. K. Lin, Q. H. Lin, and M. Angelopoulos, "Small Angle Neutron Scattering Measurements of Nanoscale Lithographic Features," J. Appl. Phys., 88, 7298 (2000).

# Electrical-Based Dimensional Metrology and Critical Dimension Reference Material Development

## Goals

Develop test-structure-based electrical metrology methods and related reference materials with emphasis on developing physical standards for tool calibration; contribute to standards organizations supporting the development of metrology standards for the semiconductor industry; target the specific near-term goal of fabricating a quantity of reference-features with nominal critical dimensions (CDs) in the range 40 nm to 240 nm and having $2\sigma$ (expanded CD uncertainties) of less than 2 nm by July 2006.

## Customer Needs

The Semiconductor Industry Association's (SIA's) International Technology Roadmap for Semiconductors *(ITRS), 2003 p. 40,* states that it is critically important to have suitable reference materials for lithography support available when on-wafer measurements are made as a new technology generation in integrated circuit (IC) manufacturing is introduced, and particularly during development of advanced materials and process tools. Each generation of ICs is characterized by the transistor gate length whose control to specifications during IC fabrication is a primary determinant of manufacturing success. The SIA projects the decrease of gate linewidths used in state-of-the-art IC manufacturing from present levels to 25 nm for the 65 nm node. Scanning electron microscopes (SEMs) and other systems used for traditional linewidth metrology exhibit measurement uncertainties exceeding *ITRS* specifications for these applications. It is widely believed that these uncertainties can be at least partially managed through the use of reference materials with linewidths traceable to nanometer-level uncertainties. Until now, such reference materials have been unavailable because the technology needed for their fabrication and certification has not been available.

## Technical Strategy

The technology that the project staff has developed for fabricating linewidth and overlay reference materials is known as the Single-Crystal CD Reference-Material (SCCDRM) implementation. Patterning SOI device layers with lattice-plane selective etches of the kind used in silicon micro machining provides reference features with quasi-atomically planar sidewalls. This unique attribute is highly desirable for the intended applications, particularly if the quasi-atomically planar sidewall smoothness can be further extended to reference-feature segment lengths of up to 2 micrometers. Essential elements of the technology implementation include starting silicon SOI (Silicon on Insulator) wafers having a (110) orientation; alignment of the reference features to specific lattice vectors; and lithographic patterning with lattice-plane selective etches of the kind used in silicon micro-machining.

The traceability path for dimensional certification originates with High-Resolution Transmission Electron Microscopy (HRTEM) imaging. This method provides nanometer-level accuracy, but is totally destructive and thus is not practical for supplying reference features to end users. The project's traceability strategy now features state-of-the-art Atomic-Force Microscopy (AFM) as a transfer metrology. Since use of available and qualified AFM tools is very costly due to the heavy demand of other metrology applications, an elaborate candidate-reference-feature selection protocol has been established. Multiple reference features on a large set of as-patterned chips are identified initially by high-power optical inspection. This procedure checks primarily for reference-feature continuity, cosmetics, and apparent uniformity of the narrowest-drawn features on the test chip which are replicated by the i-line imaging process. Drawn feature linewidths range from 350 nm to 600 nm and the "process bias" typically decreases these to replicated-CDs of between 50 nm and 300 nm. The "best" 10 % of the features passing optical inspection, and having estimated replicated CDs in the range 50 nm to 200 nm, are then SEM-imaged at 20KX. Lateral profiles of the CDs of the captured top-down SEM images are then extracted from them at 25 nm pitch. The measurements are transferred to a custom-designed database, which is then interrogated to identify sets of chips, and the reference-features on them, that are the most uniform at the narrower CDs

**Technical Contact:**
Michael W. Cresswell

***I would like to thank you and NIST for your pioneering work on silicon pocket wafer technology. We have now incorporated this technology in one of our products. We also regard very highly your work on the single crystal linewidth standard. We see this as the first and only attempt by anyone in the world to produce a linewidth standard traceable to the fundamental units of measure, in the sub-100 nm range, for use in the semiconductor industry.***

***This work is of technical and economic importance to the semiconductor industry, because the ability to correctly size ever smaller lateral dimensions on silicon substrates is key to the manufacturing yield of silicon chips.***

***We look forward to a continuing technical relationship between VLSI Standards and NIST."***

*Marco Tortonese, Ph.D., Engineering Manager,*
*VLSI Standards, Inc.*

– typically less than 150 nm. Candidate reference-features so identified on chip are CD-profiled by AFM. The AFM CD-profiles of several features on each chip are examined and the chips are then partitioned into a *calibration* sub-set and a *product* subset.

Scatterometer and OCD (Optical CD) gratings and electrical CD test structures are among the various other patterns on the test chip now being used for CD reference-feature fabrication, Fig. 1. However, the subject of all chip- and feature-selection criteria for SCCDRM transfer metrology has recently become based on some special structures called "HRTEM targets." There are several hundred of these on each chip. Their design allows the capture of six HRTEM images in a single dual-beam FIB-and-thinning operation, Fig. 2a, Fig. 2b, and Fig. 2c.

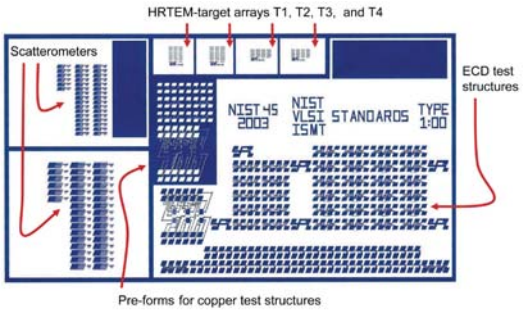


*Figure 1. Structure groupings on upper section of NIST45 SCCDRM Chip including HRTEM-target arrays T1, T2, T3, and T4.*

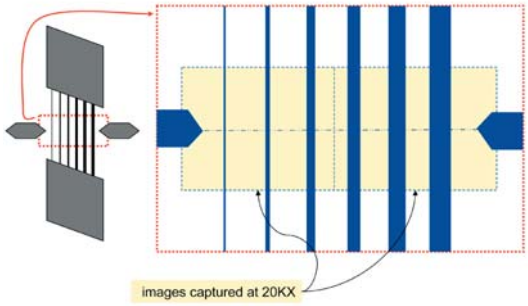


*Figure 2a. The new HRTEM-Target Layout provides images from six features having different drawn linewidths from a single FIB cut at precisely known locations along the segment lengths.*

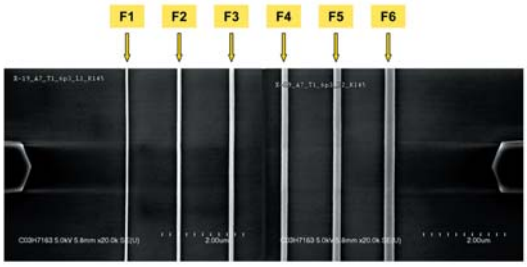


*Figure 2b. Composite of two 20KX SEM images of an HRTEM Target with annotated feature numbers. The FIB cut is made between the extremities of the markers on either side of the reference-feature grid.*

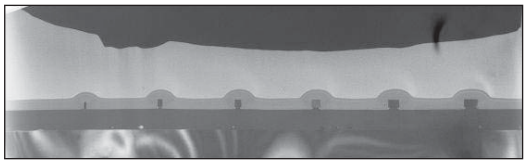

*Figure 2c. Low-magnification TEM cross-section of all six features of an HRTEM target.*

Since such operations are very costly, this capability is financially advantageous. Moreover, since the features on each target are designed such that they are systematically staggered in CD by increments of 30 nm, HRTEM inspection of a single target enables the generation of a 6-point calibration curve.

An important measure of the progress and success of the project is the level of uncertainty attributed to the product CD reference features. A composite 2-target 12-point calibration curve, from which the sub-4 nm uncertainties attributed to the chips that were recently delivered to SEMATECH were extracted, is shown in Fig. 3. In comparison, the units that were delivered to International SEMATECH four years ago typically exhibited in excess of 14 nm uncertainty. This uncertainty was attributed to average CD over several micrometers of reference feature. This macro uncertainty level is not necessarily of interest to the user who needs a value applicable to an order-of-magnitude less segment length. In addition, the cited uncertainty levels were considered to be four to five times higher than what is desired for the roadmap out years. Therefore, the main goal of the project during the current calendar year was reducing the uncertainty to 5 nm or better over reference-feature micro-segment lengths of the order of several tens of nanometers.

To facilitate achieving the stated goal, last year's effort was focused on reducing the macroscopic variations of the physical CDs of the reference features by refinements to the starting-material specifications and to the wafer-fabrication process. The uniformity of fabricated reference features with a nominal 100 nm dimension consequently improved to less than 2 nm per micron of reference-feature segment-length. This improvement is closely tied to the 1.5 nm to 4 nm uncertainties that was ultimately attributed to features on chips comprising the recent delivery.

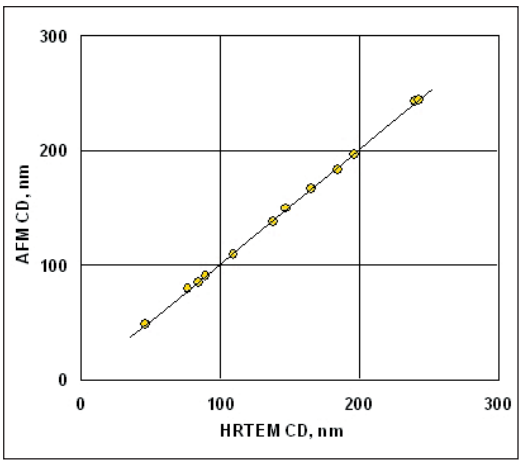


*Figure 3. "Example of AFM Transfer-Calibration from a single HRTEM target."*

Since 200 mm (110) starting material is virtually unobtainable at an acceptable cost, this project's technical strategy has been to dice each 150 mm (110) wafer after lithography and to mount the separate chips in micro-machined standard 200 mm wafers to accommodate the product reference-feature chips. The result is that finished units are rendered metrology-tool-compatible at an acceptable cost. The chips that were delivered in January 2005 were mounted in 200-mm carrier wafers for distribution.

**DELIVERABLES:** Design a new reference-material test chip having multiple targets each having features with varying ranges of drawn line widths that substantially reduce the cost of HRTEM imaging. Provide new navigational tools to facilitate referencing along lengths of reference features in excess of one micrometer. Include a new segmentation mask level that partitions reference features into multiple shorter segments after patterning without adversely affecting essential reference feature properties, such as sidewall planarity, and provide all necessary on-chip navigational aids to facilitate identification of segments so produced under high-power imaging. 1Q 2006

**DELIVERABLES:** Evaluate improved reference-feature properties by locating the etch reflux systems in inert atmospheres. The motivation for this process change is to reduce the CD non-uniformity along the reference feature to sub-nanometer from present several-nanometer levels. The model is that more control of reference-feature sidewall-surface cooling, and the ambient to which it is exposed during withdrawal from the hot etch solution, will result in superior CD uniformity and, ultimately, in still lower uncertainty levels. 2Q 2006

**DELIVERABLES**: Reduce reference-feature sidewall asperities by developing separate processes that target sidewall contamination by organic materials and by residual moisture. These processes may include immersion of the patterned chips in ultra-sonically agitated solvents, extensive pre-cleaning of quartz-ware, and vacuum baking. Construct a relational database to archive all measurements and processing conditions. Add report generators to rank reference features on the basis of measured properties such as CD uniformity, both lateral (along the feature) and vertical (from base of feature to its top surface.) 3Q 2006

**DELIVERABLES**: Design and perform an experiment to identify the factors that affect the fabrication and cleaning of silicon test features with nano-scale CDs. Eight factors that are known to be potentially-important have been identified and their effects on the test features will be compared on the bases of yield, cleanliness, uniformity and narrowness of feature linewidth. 2Q 2006

**DELIVERABLES:** Select reference features on a set of 30 chips that are judged to have superior potential for providing sub-40 nm CDs with sub-2 nm expanded uncertainties. Select a sub-set of 3 chips to be submitted for HRTEM imaging to establish an 18-point calibration curve for referencing AFM measurements on the other 27 chips to the to lattice-spacing-based absolute measurements. 4Q 2006

**DELIVERABLES:** Apply project's recently-developed protocol for extracting consistent HRTEM-CD measurements by multiple observers from the features that are submitted for imaging. Reconcile the HRTEM and AFM measurements of each respective feature on a single calibration curve for the purpose of assigning calibrated CDs and their $2\sigma$ expanded uncertainties to 10 chips that will be assembled into carrier wafers for delivery to industry clients. 4Q 2006

**DELIVERABLES:** Fabricate scatterometry targets using the single-crystal reference-material implementation. Invite industry partners to evaluate performance. 4Q 2005

## Accomplishments

■ *A selection of SIMOX (Separation by IMplantation of Oxygen) (110) 150 mm wafers was procured, pre-processed by p-dopant implantation and annealing, and circulated between outside contractors for implantation, hard-mask deposition, and lithography.* After lithography,

the wafers with patterned hard-mask films were delivered to NIST for dicing prior to their being patterned at the chip level and inspected by optical and SEM microscopy. During this period, a prototype cleaning process was developed to eliminate particulate and chemical contamination that formerly severely limited the features' usefulness. This procedure was generally successful in preventing 'skipping' of the CD-AFM boot-tip probe, which was essential for AFM imaging. However, it appears that further development of this cleaning process would be advantageous as far as totally removing the SEM-induced hydrocarbon contamination and/or all other residues that are sometimes left on the reference-features' surfaces after patterning.

■ *As a consequence of implementing the wafer-processing improvements described above, and in collaboration with SEMATECH, VLSI Standards, Inc., and Accurel Systems, Inc., the uncertainties attributed to critical dimension (CD) reference features having calibrated CDs in the range of 40 nm to 100 nm were significantly improved.* The improvement in uncertainty results from further technical innovations such as the implementation of a new type of HRTEM-imaging (High-Resolution Transmission Electron Microscopy) test structure, the extensive use of SEM (Scanning Electron Microscope) inspection to identify targets with superior CD uniformity, and the introduction of CD-AFM (CD-Atomic Force Microscopy) to serve as the transfer metrology. A selection of the reference materials was distributed to SEMATECH Member Companies for evaluation.

■ *Questionnaires Distributed, Workshop Held, News Release Issued, and Papers Presented*: These activities were undertaken to contribute to orderly and effective Technology Transfer to industry of the project's outputs. A questionnaire on the use and usefulness of the SCCDRMs that were distributed to SEMATECH member companies was compiled and distributed to the recipients. A proportion has already been returned and the remainder are being actively sought with the assistance of SEMATECH as the summary results are being compiled. A Workshop, which was open to the public, was co-sponsored by NIST and SEMATECH to inform the general public of the availability of sample SCCDRMs. It was held in conjunction with a major semiconductor technical conference and trade show in San Jose, California, in March 2005. The workshop was pre-announced in News Release issued by NIST after which approximately 12 different trade-magazine editors interviewed project engineers and published their own reports. These were generally complimentary and upbeat. This year alone, Project engineers have made no fewer than five conference presentations. One conference has asked for a new paper from us for an upcoming special issue of the IEEE Transactions on Semiconductor Manufacturing.

■ *ATP Program Award:* The Project engineering team, which is drawn from three different OUs at NIST, bid on, and was awarded, a $1.5M program to produce a third generation of SCCDRM artifacts.

## FY Outputs

### Collaborations

■ NIST MEL: Development of AFM CD-profile extraction

■ NIST ITL: Traceability statistics and procedures

■ Accurel Systems: Design of HRTEM targets and formulation of appropriate imaging procedures.

■ The Scottish Microelectronics Centre at the University of Edinburgh, U.K. We are collaborating with this organization, which has received other-agency funding for the purpose of working with us on this project. Their principal contribution at this time is wafer fabrication and related technical contributions.

### Standards Committee Participation

■ Electrical Test Structures Task Force, Co-Chair (Richard A. Allen)

■ SEMI International Standards Micro-lithography Committee, member (Richard A. Allen)

## Recent Publications

R. A. Allen, M. W. Cresswell, C. E. Murabito, W. F. Guthrie, L. W. Linholm, C. H. Ellenwood, E.H. Bogardus, "Test Structures for Referencing Electronics Linewidth Measurements to Silicon Lattice Parameters Using HRTEM," Proceedings of the 2002 ICMTS, IEEE 2002 International Conference on Microelectronic Test Structures, Apr 09-11, 2002, Cork, Ireland, pp. 13-18, (08-APR-2002).

B. A. am Ende, M. W. Cresswell, R. A. Allen, T. J. Headley, W. F. Guthrie, L. W. Linholm, E. H. Bogardus, C. E. Murabito, "Measurement of the Linewidth of Electrical Test-Structure Reference Features By Automated Phase-Contrast Image Analysis," Proceedings of the 2002 ICMTS, IEEE 2002 International Conference on Microelectronic Test Structures, Cork, Ireland, Vol. 15, pp. 1-5, (01-APR-2002).

M. W. Cresswell, E. H. Bogardus, J. V. Martinez de Pinillos, M. H. Bennett, R. A. Allen, W. F. Guthrie, C. E. Murabito, B. A. am Ende, L. W. Linholm, "CD Reference Materials for Sub-Tenth Micrometer Applications," Proceedings of the SPIE, SPIE's 27th Annual International Symposium and Education Program on Microlithography, Mar 03-08, 2002, Santa Clara, California, Vol. 4689, pp. 116-127, (01-JUN-2002).

R. Schlaf, Y. Emirov, J. A. Bieber, A. Sikder, J. Kohlscheen, D. A. Walters, M. R. Islam, B. Metha, Z. F. Ren, T. L. Shofner, B. B. Rossi, M. W. Cresswell, "Using Carbon Nanotube Cantilevers in Scanning Probe Metrology," Proceedings of the SPIE, SPIE's 27th Annual International Symposium and Education Program on Microlithography, Mar 03-08, 2002, Santa Clara, California, p. 53, (01-JUN-2002).

R. Schlaf, Y. Emirov, J. A. Bieber, A. Sikder, J. Kohlscheen, D. A. Walters, M. R. Islam, B. Metha, Z. F. Ren, T. L. Shofner, B. B. Rossi, M. W. Cresswell, "Using Carbon Nanotube Cantilevers in Scanning Probe Metrology," Proc. Intl. Soc. for Optical Engineering (SPIE), SPIE - The International Society for Optical Engineering, Mar 03-08, 2002, Santa Clara, California, pp. 53-53 (01-JUN-2002).

R. A. Allen, R. I. Patel, M. W. Cresswell, C. E. Murabito, B. Park, M. D. Edelstein, L. W. Linholm, "Recent Developments in Producing Test-structures for Use as Critical Dimension Reference Materials," ICMTS IEEE International Conference on Microelectronic Test Structures, Mar 22-25, 2004, Awaji, Japan, pp. 35-40 (01-MAR-2004).

R. A. Allen , M. W. Cresswell, C. E. Murabito, R. Dixson, E.H. Bogardus, "Critical Dimension Calibration Standards for ULSI Metrology," Characterization and Metrology for ULSI Technology: 2003, International Conference on Characterization and Metrology for ULSI Technology, Mar 24-28, 2003, Austin, Texas, pp. 421-428 (30-SEP-2003).

R. A. Allen, B. A. am Ende, M. W. Cresswell, C. E. Murabito, T. J. Headley, W. F. Guthrie, L. W. Linholm, C. H. Ellenwood, E.H. Bogardus, "Test Structures for Referencing Electrical Linewidth Measurements to Silicon Lattice Parameters Using HRTEM," IEEE Transactions on Semiconductor Manufacturing, Vol. 16, No. 2, pp. 239-248 (01-MAY-2003).

R. A. Allen , M. W. Cresswell, L. W. Linholm, " Junction-Isolated Electrical Test Structures for Critical Dimension Calibration Standards," 2003 ICMTS IEEE International Conference on Microelectronic Test Structures, Mar 17-20, 2003, Monterey, California, pp. 3-7 (31-MAR-2003).

N. Guillaume, M. Lahti, M. W. Cresswell, R. A. Allen , L. W. Linholm, M. E. Zaghloul, "Non-contact Electrical Critical Dimensions Metrology Sensor for Chrome Photomasks," Proc. Intl. Soc. for Optical Engineering (SPIE), 21st Annual BACUS Symposium on Photomask Technology, Oct 02-05, 2001, Monterey, California, Vol. 4562, pp. 822-829 (01-OCT-2002).

M. W. Cresswell, E.H. Bogardus, J. V. Martinez, M. H. Bennett, R. A. Allen, W. F. Guthrie, C. E. Murabito, B. A. am Ende, L. W. Linholm, "CD Reference Materials for Sub-Tenth Micrometer Applications," Proc. Intl. Soc. for Optical Engineering (SPIE), SPIE - The International Society for Optical Engineering, Mar 03-08, 2002, Santa Clara, California, Vol. 4689, pp. 116-127 (01-JUN-2002).

R. A. Allen, M. W. Cresswell, C. E. Murabito, W. F. Guthrie, L. W. Linholm, C. H. Ellenwood, E.H. Bogardus, "Test Structures for Referencing Electronics Linewidth Measurements to Silicon Lattice Parameters Using HRTEM," Proc., 2002 ICMTS, IEEE 2002 International Conference on Microelectronic Test Structures, Apr 09-11, 2002, Cork, United Kingdom, pp. 13-18 (08-APR-2002).

B. A. am Ende, M. W. Cresswell, R. A. Allen , T. J. Headley, W. F. Guthrie, L. W. Linholm, E.H. Bogardus, C. E. Murabito, "Measurement of the Linewidth of Electrical Test-Structure Reference Features By Automated Phase-Contrast Image Analysis," Proc., 2002 ICMTS, IEEE 2002 International Conference on Microelectronic Test Structures, Cork, United Kingdom, Vol. 15, pp. 1-5 (01-APR-2002).

J. von Hagen, H. A. Schafft, "Temperature Determination Methods on Copper Material for Highly Accelerated Electromigration Tests (e.g., SWEAT)," 2002 IEEE International Integrated Reliability Workshop Final Report, 2002 Integrated Reliability Workshop, Oct 21-24, 2002, Lake Tahoe, California, pp. 45-49 (01-FEB-2003).

H. A. Schafft, J. R. Lloyd, "Electromigration Discussion Group Summary," 2002 IEEE International Integrated Reliability Workshop Report, 2002 IEEE International Integrated Reliability Workshop, Oct 21-24, 2002, Lake Tahoe, California, pp. 204-206 (01-FEB-2003).

H. A. Schafft, L. M. Head, J. Gill, T. D. Sullivan, "Early Reliability Assessment Using Deep Censoring," Microelectronics Reliability, Vol. 2003, No. 43, 16 pp. (01-JAN-2003).

"Establishing Traceability of Linewidth Reference Materials Using CD-AFM and HRTEM," W.F. Guthrie1, R.G. Dixson, R.A. Allen, M.W. Cresswell, C.E. Murabito, B. Park 2005 International Conference on Characterization and Metrology for ULSI Technology, March 15-18, 2005, University of Texas at Dallas.

R. A. Allen, A. Hunt, C. E. Murabito, B. Park, W. F. Guthrie, and M. W. Cresswell, "Extraction of Critical Dimension Reference Feature CDs from New Test Structure Using HRTEM Imaging," Proceedings of the 2005 IEEE International Conference on Microelectronic Test Structures, pp. 5- 10, March 2005, Leuven, Belgium.

R. G. Dixson, M. W. Cresswell, W. F. Guthrie, R. A. Allen, "CD-AFM Reference Metrology at NIST and International SEMATECH," to be published in SPIE Proceedings Vol. 5752 (2005).

"Report of Investigation of RM 8111: Single-Crystal Critical Dimension Prototype Reference Materials," National Institute of Standards and Technology, Gaithersburg, Maryland, March 2, 2005.

"CD Reference Features with Sub-Five Nanometer Uncertainty" M. W. Cresswell, R. G. Dixson, W. F. Guthrie, R. A. Allen, C. E. Murabito, B. Park, J. V. Martinez de Pinillos, and A. Hunt to be published in SPIE Proceedings Vol. 5752 (2005).

# Optical-Based Photomask Dimensional Metrology

**Technical Contact:**
R. Silver
J. Potzick
T. Doiron

## Goals

Provide technological leadership to semiconductor and equipment manufacturers and other government agencies by developing and evaluating the methods, tools, and artifacts needed to apply optical techniques to the metrology needs of semiconductor microlithography. One specific goal is to provide the customer with the techniques and standards needed to make traceable dimensional measurements on photomasks and wafers, where appropriate, at the customer's facility. The industry focus areas of this project are primarily the optical based methods used in overlay metrology, photomask critical dimension metrology, and high-accuracy two-dimensional placement metrology.

## Customer Needs

Tighter tolerances on CD measurements in photomask and wafer production place increasing demands on photomask linewidth accuracy. NIST has a comprehensive program to both support and advance the optical techniques needed to make these photomask critical dimension measurements.

Improved two-dimensional overlay measurement techniques and standards are needed for measuring and controlling overlay capabilities of steppers and separating out the contributions from the photomask. Overlay is listed in Table 115 of the 2003 SIA ITRS as a difficult challenge for <45 nm processes. Overlay improvements have not kept pace with resolution improvements and will be inadequate for ground rules less than 45 nm. In fact, Table 117b shows that no known solutions for overlay output metrology exist beyond the 65 nm node. As shown in Table 117a, the problems are more acute for CD metrology where the industry is currently encountering metrology problems without known manufacturing solutions.

## Technical Strategy

There are two main strategic technical components of this project.

1. Photomask linewidth measurements using the ultraviolet transmission microscope, calibration of NIST Photomask Linewidth Standard SRM 2059, and the development of calibration methods to obtain photomask linewidth measurement uncertainties adequate to meet industry needs.

The technical strategy for photomask linewidth standards is divided into two segments: (1) instrumentation and model development and (2) design and calibration of standard artifacts. An ultraviolet transmission microscope (Fig. 1) has been constructed which uses a unique geometry (a Stewart platform) as the main rigid structure. This microscope platform has good vibration characteristics and presents an open mechanical architecture. Higher image resolution, reduced transmission of UV light through the chrome, and reduced instrument vibration offer improved linewidth measurement uncertainties.

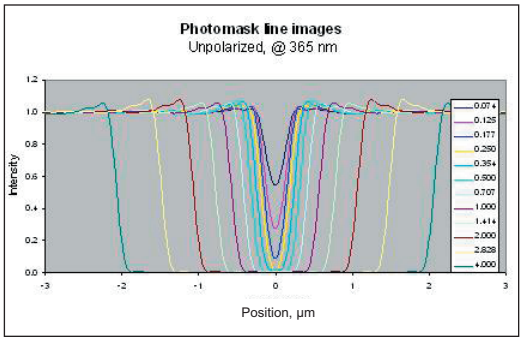


*Figure 1. Modeling results for linewidth photomask samples showing CDs down to 0.25 µm.*

NIST has supplied a substantial number of photomask linewidth standards worldwide over the past decade. Chrome-on-quartz photomasks with linewidth and pitch features in the range of 0.5 µm to 30 µm have been certified on the previous NIST green light optical calibration system. Linewidth uncertainties have been reduced to 20 nm, k=2. The next generation in this line of standards is SRM 2059 (Fig. 2), printed on a standard size $1.4 \times 10^{-4}$ $cm^3$ substrate with calibrated linewidths and space-widths ranging from nominally 0.25 µm to 32 µm, and pitch patterns from 0.5 µm to 250 µm.

In response to customers' needs for more accurate photomask feature size measurements, NIST has worked extensively to improve mask metrology through modeling and improved optical microscope characterization methods. The features on even the highest quality masks exhibit roughness and runout at the chrome edges, compromising

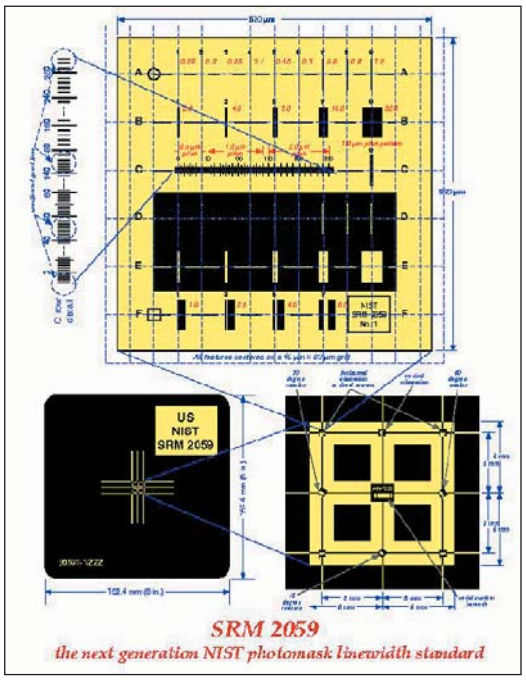


*Figure 2. The new linewidth photomask standard.*

the definition of edge and linewidth. Modeling the effects of all of the relevant feature properties in both the mask metrology process and in wafer exposure and development processes, using existing and new software tools, can improve feature size accuracy by establishing accurate simulation results and improving the relationship between mask-feature metrology and the corresponding wafer-feature sizes.

**DELIVERABLES:** Compare and improve the accuracy of the NIST optical scattering code with new scattering models developed by Spectel and Panoramic Technologies for use in transmission. 3Q 2005.

2. The second major component is the development of two-dimensional grid calibration standards and associated measurement techniques, including statistical analysis and charge-coupled device (CCD) characterization as used by industry. These individual technical strategies for these components are described next.

We are approaching the problem of two-dimensional measurements from a couple of directions. The first is the calibration of an artifact standard which can be used to bring all of the two-dimensional based inspection instruments to the same metric. This work has developed a standard grid which is now available as a NIST Standard Reference Material, # 5001. The artifact can be used by the semiconductor industry to standardize 2-D measurements. The SRM 5001 was developed as an industry consensus standard grid and calibrated with measurements on a state-of-the-art industry machine followed by verification of the measurements using NIST Linescale Interferometer capabilities which resulted in traceable two-dimensional measurements..

A new generation of grid for the SRMs has been fabricated and another round of measurements is in process. Each measurement of the grid has data in each of at least two orientations. Rotating the grid 90° between measurements samples a number of the geometric errors of the machine. The remaining geometric sources of uncertainty are the scale and some components of the linearity of each machine axis travel.

Verification of the industry-based grid measurements is done at NIST. The overall scale of the grid is checked with the NIST linescale interferometer, an instrument that is known to provide the most accurate 1-D measurements available in the world. Two sources of uncertainty not captured by these measurements include components of the straightness and effects of the plate bending when fixtured. Work is now focused on the new Nikon5i two-dimensional metrology tool at NIST. The Nikon 5i has been fully characterized and is now in a calibration verification sequence for use in future grid calibrations.

To strengthen the foundation of NIST's linewidth measurement traceability and to support the Bureau International des Poids et Mesures (BIPM) *Mutual Recognition Arrangement*, NIST has become the pilot laboratory for an international intercomparison of submicrometer linewidth measurements. National metrology institutes in nine countries around the world are participating.

**DELIVERABLES:** Use a new advanced algorithm to flag automated focus and positioning control system errors to improve measurement system performance. Continue to develop comprehensive analysis capabilities for centerline and edge detection methods. 2Q 2005.

**DELIVERABLES:** Implement the standard scale correction and new mapping software for the Nikon 5I system. Measure the new set of two-dimensional calibration grids with a complete uncertainty. 4Q 2005.

**DELIVERABLES:** Complete the second round of calibrations of SRM 2059 and complete the related documentation. Deliver the accompanying documentation to the Office of Standard Reference Materials for distribution to customers. 3Q 2005.

## Accomplishments

■ ***SRM 2800 Microscope Magnification Standard*** is a standard-size microscope slide with calibrated pitch features ranging from 1 μm to 1 cm (see Fig. 3). It contains a lithographically produced chrome pitch pattern consisting of a single array of parallel lines with calibrated center-to-center spacings. It contains no linewidth structures. This SRM is intended to be used for the calibration of reticles and scales for optical or other microscopes at the user's desired magnification. The SRM may be used in either transmission or reflection mode optical microscopes, SEMs, or SPMs. Calibration is traceable to the meter through NIST Line Scale Interferometer. Fifty-six units have been calibrated and delivered to the NIST Office of Standard Reference Materials and nearly half of current stock has been sold.

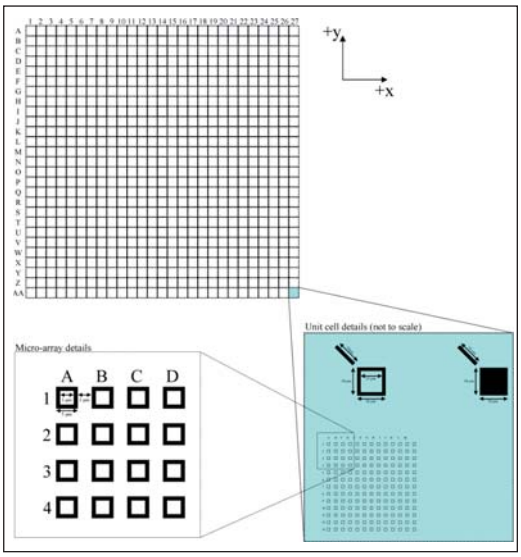


*Figure 3. The two dimensional grid photomask standard, now available through the SRM office.*

■ NIST currently is completing the uncertainty analysis and documentation for *SRM 2059 Photomask Linewidth Standard*, which will enable customers to make traceable measurements of the dimensions of features on integrated circuit photomasks.

■ The first set of two-dimensional grid artifacts, known as SRM 5001, and has been calibrated and delivered to the SRM office. These 6-inch photomasks have been measured on a state-of-the-art I-pro metrology system by the photomask manufacturer. A second set of re-designed 6-inch feature placement standards has been fabricated and measured in the close collaboration between NIST and Photronics. The collaboration employs the industry tool and the traceability of the NIST line scale interferometer with appropriate statistical analysis (see Fig. 4). The uncertainty budget for grid measurements has been completed.

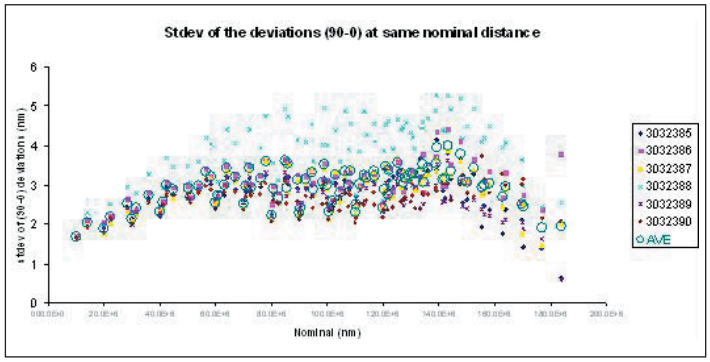


*Figure 4 shows tool repeatability and mapping data for the two-dimensional mask calibration procedure.*

■ Work closely with SEMATECH to complete a comprehensive report using optical methods for the calibration of phase shifting photomasks. This includes modeling and measurements in transmission and reflection.

## Collaborations

ISMT, IBM, IVS Schlumberger, KLA-Tencor, Intel, Motorola, AMD and several other leading manufacturers or tool vendors.

The 14 members of The Neolithography Consortium.

## Recent Publications

J. M. Pedulla, J. Potzick*, R. Silver*, and R. Larrabee, "Improving the Uncertainty of Photomask Linewidth Measurements," SPIE Vol. 5375, p. 317, 2004.

J. Potzick, J.M. Pedulla, M. Stocker, "Updated NIST Photomask Linewidth Standard," Proceedings of SPIE 28th International Symposium on Microlithography, vol. 5038-34 (2003).

R. M. Silver, R. Attota, M. Stocker, J. Jun, E. Marx, R. Larrabee, B. Russo, and M. Davidson, "Comparison of Measured Optical Image Profiles of Silicon Lines with Two Different Theoretical Models," Metrology, Inspection and Process Control for Microlithography XVI, Proc. SPIE, Vol. 4689, p. 409, 2002.

R. M. Silver, J. Jun, E. Kornegay and R. Morton, "Comparison of Edge Detection Methods using a Standard Prototype Overlay Calibration Artifact," Proc. SPIE Vol. 4344, p. 515 (2001).

J. Potzick, "The problem with submicrometer linewidth standards and a proposed solution," *Proceedings of SPIE 26th International Symposium on Microlithography*, vol. 4344-20 (2001).

S. Fox, “Focus, edge detection and CCD camera characterization for development of an optical calibration standard,” University of Maryland, PhD Thesis 2000.

T. Doiron and R. Silver, “Two-dimensional grid Standards,” Proc. Measurement Sciences Conf. (2000).

S. Fox, E. Kornegay, and R. Silver, “Characterization of Imaging Optics and CCD Cameras for Metrology Applications,” *Characterization and Metrology for ULSI Technology*, D. Seiler, et. al., eds, A.I.P. Press, 2000, pp. 378-382.

S. Fox, R. Silver Thesis Advisor, “Focus, Edge Detection, and CCD Camera Characterization for Development of an Optical Overlay Calibration Standard,” Graduate Thesis, Univ. of MD (2000).

J. Potzick, “The Neolithography Consortium—a progress report,” *Proceedings of BACUS Symposium on Photomask Technology*, vol. 4186-73 (2000).

J. Potzick, “The Neolithography Consortium,” *Proceedings of SPIE 25th International Symposium on Microlithography*, vol. 3998-54 (2000).

M. Schroeck, and T. Doiron, “Probing of two-dimensional grid patterns by means of camera based image processing,” accepted by SPIE for January 2000.

K. Meissner, and T. Wegener, “Robust Regression for Two Dimensional Coordinate Measurements,” Proceedings of the International Symposium on Laser Metrology for Precision Measurement and Inspection in Industry, Florianoplis, Brazil, October 13-15, 1999.

R. Silver, T. Doiron, S. Fox, E. Kornegay, M. Takac, and S. Rathjen, Two dimensional Grid Standards, Proceedings of the SPIE, The International Society for Optical Engineering, Metrology, Inspection, and Process Control for Microlithography XIII (1999).

# Model-Based Linewidth Metrology

## Goals

The goal of this project is to address the metrology needs of industry, particularly the U.S. semiconductor industry, for linewidth metrology with uncertainties of a few nanometers.

## Customer Needs

*"Stack materials, surface condition, line shape and even layout in the line vicinity may affect CD-SEM waveform and, therefore, extracted line CD. These effects unless they are accurately modeled and corrected increase measurement variation and, therefore, total uncertainty of CD-SEM measurements."* **International Technology Roadmap for Semiconductors, Metrology Section, p. 7 (2003).**

*"Due to the changing aspect ratios of IC features, besides the traditional lateral feature size, e.g. linewidth measurement, full three-dimensional shape measurements are gaining importance and should be available inline. Development of new metrology methods that use and take the full advantage of advanced digital image processing and analysis techniques, telepresence, and networked measurement tools will be needed to meet the requirements of near future IC technologies."* **International Technology Roadmap for Semiconductors, Metrology Section, p. 6 (2003).**

*"…the exponential rise in value of each nanometer, as nominal gate dimensions shrink, can be estimated… Under these assumptions, the value of CD control for the 180 nm generation of microprocessors exceeds $10 per nanometer."* **C.P. Ausschnitt and M. E. Lagus, IBM Advanced Semiconductor Technology Center, Proc. SPIE Vol. 3332, p. 212 (1998).**

A feature's width is one of its fundamental dimensional characteristics. Width measurement is important in a number of industries including the semiconductor electronics industry, which had approximately $213 billion in worldwide sales in 2004.[1] As a measure of its importance in that industry, consider that the term "critical dimension" or "CD" is used there nearly interchangeably with "linewidth," and semiconductor device generations are known according to the characteristic width of the features, as in "the 65 nm technology node."

To support present and future semiconductor technologies, industry needs to measure gate widths with total uncertainties, as identified in the International Technology Roadmap for Semiconductors (ITRS), of less than 3 nm and with measurement repeatabilities of better than 0.6 nm. Neither NIST nor any other national laboratory presently offers a wafer linewidth measurement service or SRM with uncertainty at this level. In addition to measuring linewidths, the semiconductor industry has needs for measuring linewidth *variation*, that is, linewidth roughness (LWR). LWR in transistor gates has been linked to increased off-state leakage current and to threshold voltage variation. The 2003 ITRS specified that LWR, measured as three standard deviations of the CD, must be less than 2.6 nm in 2005 and be measured with better than 0.5 nm repeatability.[2]

A line's width must generally be determined from its image. However, the image is not an exact replica of the line. The scanning electron microscope (SEM), scanning probe microscope (SPM), and optical microscope all have image artifacts that are important at the relevant size scales. Physical linewidth determination therefore requires modeling of the probe/sample interaction in order to correct image artifacts and identify edge locations. Barriers to accurate linewidth determination include inadequate confidence in existing models, the complexity and consequent expense of using some models, inadequately quantified methods divergence, and ignorance of best measurement practices. Barriers to accurate LWR measurement include poorly understood measurement artifacts such as measurement bias that comes from treating random edge assignment errors as a component of roughness (a false "noise roughness") and random errors due to noise or sampling.

## Technical Strategy

The scope of the model-based linewidth metrology project includes the development and improvement of computational models to simulate

[1] Semiconductor Industry Association press release, January 31, 2005.

[2] The 2004 update omits a LWR specification, saying only that a proposed new definition for LWR is under consideration.

**Technical Contact:**
John Villarrubia

***"[The] theoretical work on the behavior of the probe-sample interaction has had a profound influence on our ability to quantitatively analyze probe microscope images."***

*Joseph Griffith, Bell Labs, Lucent Technologies*

***"The modeling work … for electrical CD, AFM, and CDSEM is of value to us ... The current crisis in CD offset uncertainty may be partially answered by this work."***

*Anonymous industry feedback to NIST*

the artifacts introduced by measuring instruments, inversion of these models (to the extent possible) to deduce the sample geometry that produced a measured image, validation of models by appropriate experiments, development and testing of measurement processes that provide the necessary inputs for model-based deduction of sample width and shape, estimation of uncertainties for the measurement process, assistance to industry linewidth measurement by communication of best practices, and laying of the necessary research groundwork for a future linewidth and/or line shape Standard Reference Material.

We have been developing a model-based library method of determining linewidth and line shape from top-down SEM images. The top-down measurement configuration is the one employed by industry CD-SEMs. Edge locations tell us the line's width (the "CD" desired by industry). However, lines with different sidewall geometries appear to have different widths when measured using algorithms that are standard today on CD-SEMs. That is, sidewall variation masquerades as width variation. Accordingly, our method is a model-based algorithm that explicitly accounts for the physics of the interaction of the electron beam with the sample and the effect of sidewall geometry.

The method works like this: A set of parameters for describing edge geometry is chosen. These parameters might be, for example, sidewall angle and corner radius. For a given set of parameter values, the expected image is calculated using a Monte Carlo algorithm that simulates electron trajectories. This calculation is repeated for other choices of edge parameters at discrete intervals representative of the range of shapes that one is likely to encounter in a measurement. The resulting actual shape / calculated image pairs form a library, or database. To determine the shape of an unknown sample, its measured image is compared to computed images in the database to find the closest match. The corresponding line shape is assigned to the unknown (Fig. 1). In practice there may be more than two parameters, and the library may be interpolated.

In recent years we have reported encouraging results for this method. Results for polycrystalline Si are shown in Fig. 2a and Fig. 2b. Measurements like these on poly-Si are industrially relevant after etch, and are also important as a prerequisite for the calibration of wafer linewidth standards. Such standards are likely to be fab-

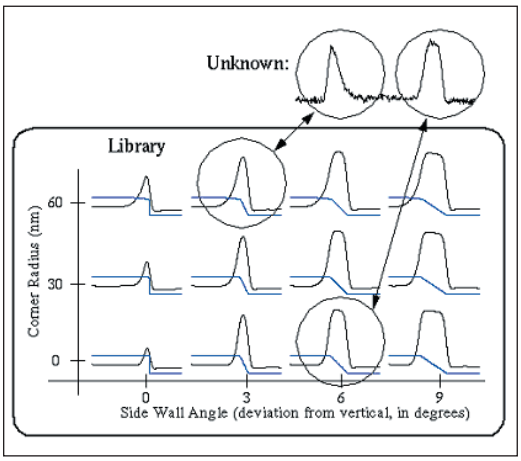


*Figure 1. Concept of metrology using a model-based library. The measured left and right edges are compared to a library of images calculated for a range of possible edge shapes. The shape of the unknown structure that gave rise to the measured image is assigned to be the line shape corresponding to the image that most closely matches the measured one.*

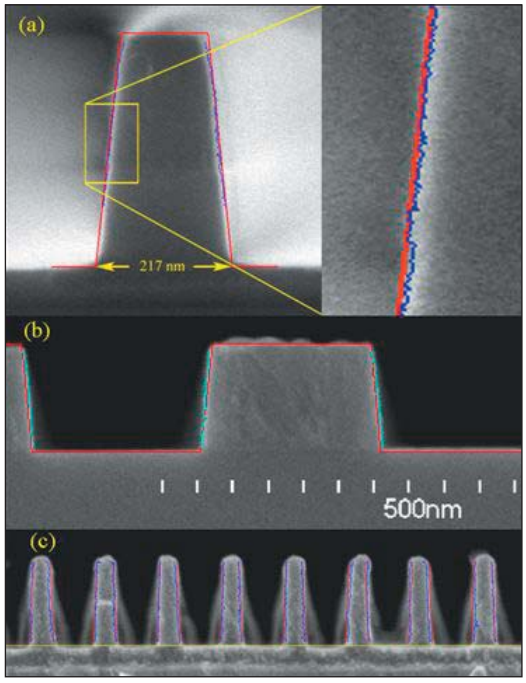


*Figure 2. Agreement between MBL and cross-section measurements (a) for isolated polycrystalline ("poly") Si lines in which top-down measurements were performed with a laboratory SEM, (b) for dense poly lines measured with a commercial CD-SEM, and (c) for dense UV resist lines measured with a commercial CD-SEM. In all cases the red lines are the cross sections predicted by the MBL technique based upon top-down measurements, and the blue lines are edges assigned based upon the cross sections (See "Recent Publications" 1, 2, & 3).*

ricated in Si rather than resist because resist geometry is too unstable for a long-term standard. However, a capability to measure resist would also be industrially useful for pre-etch process control measurements. The effects of contamination, charging, and shrinkage when imaging nonconducting resists may result in poorer accuracy for resist samples than for Si samples. Results for a UV resist were obtained in 2003 and are shown in Fig. 2c. One manufacturer of CD-SEMs is now marketing a microscope, announced in summer 2003 at SEMICON WEST, with their own implementation of a MBL method. Others are investigating the method.

In 2005 we are improving the capabilities of the underlying modeling tools used to generate libraries. The existing simulation codes are limited to certain classes of sample shapes, essentially lines uniform along their length and with cross sections characterized by a small number of geometrical parameters, *e.g.*, width, sidewall angle, and corner radius. Improvements to the modeling code would permit simulation of other industrially important sample shapes, such as rough-edged lines, contact holes, and line footing. We are also encouraging further adoption of this method by CD-SEM suppliers by further publication of the method, by making modeling software freely available to CD-SEM manufacturers, and by collaboration with their engineers.

**DELIVERABLES:** New more general sample shapes will be added to those capable of being simulated by NIST's MONSEL Monte Carlo SEM modeling code. These shapes will permit extending the MBL method to line edge roughness, contact holes, and other industrially relevant samples. Results will be reported 4Q 2005.

**DELIVERABLES:** Publication of a review of the method and its results in an archival journal (4Q 2005) and presentation at SPIE of a collaborative paper with a CD-SEM supplier (1Q 2005).

With regard to linewidth roughness measurement issues, we are collaborating with colleagues at International SEMATECH, where we can obtain CD-SEM images of specially fabricated test samples. Such images analyzed at NIST in late 2003 and early 2004 revealed a number of measurement artifacts when roughness is measured using standard methods. For example, noise-induced measurement bias was determined to be significant for samples as smooth as required by the ITRS (see the upper, "standard metric" curve in Fig. 3). In 2005 we are investigating a proposed alternative measurement method that is not subject to this source of bias.

**DELIVERABLES:** Presentation at SPIE (1Q 2005) and publication in its proceedings (3Q 2005) of the results of a test of our proposed unbiased LWR metric.

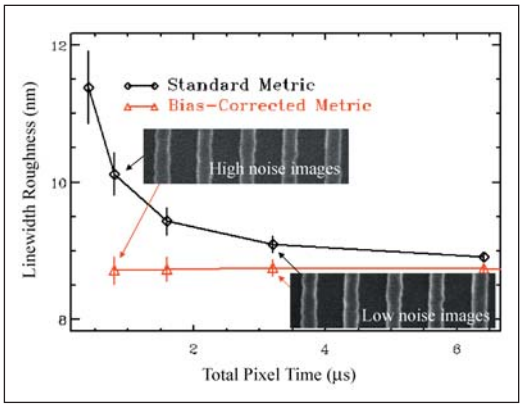


*Figure 3. Measured LWR vs. pixel integration time for two different LWR metrics. Lower pixel integration time corresponds to higher noise in the image. Vertical bars are ±1 standard deviation of the observed repeatability. These were repeated measurements at the same location—therefore all measured values ought to be the same and any observed dependence of LWR upon pixel integration time must be a measurement artifact. Figure based on "Recent Publication" 4.*

## Accomplishments

■ In cooperation with another NIST division, we organized and held an International Workshop on "Modeling Electron Transport for Applications in Electron and X-Ray Analysis and Metrology." We presented a review paper on "SEM Dimensional Metrology Using a Model-Based Library," that will be published in *Surface and Interface Analysis* (see "Recent Publications" 5).

■ In collaboration with the Production Engineering Research Laboratory of Hitachi, Ltd. (which researches CD measurement algorithms for Hitachi CD-SEMs), we compared the sensitivity of several linewidth measurement methods to SEM focus variation (see "Recent Publications" 6). The results indicated that MBL is less sensitive than the current standard methods. However, some sensitivity at large defocus was observed. This sensitivity was attributed to approximations in the beam shape model.

■ Our proposed unbiased LWR metric (lower curve in Fig. 3) performed very well in comparison to the standard metric. Results will be

published in the SPIE conference proceedings and have already been made available to CD-SEM suppliers (see "Recent Publications" 4).

## Collaborations

International SEMATECH, Benjamin Bunday, Michael Bishop.

Hitachi, Ltd., Maki Tanaka.

## Recent Publications


1. "Scanning electron microscope analog of scatterometry," J. S. Villarrubia, A. E. Vladár, J. R. Lowney, and M. T. Postek, *Proc. SPIE* **4689**, pp. 304-312 (2002).

2. "Test of CD-SEM Shape-Sensitive Linewidth Measurement," J. S. Villarrubia, A. E. Vladár, and M. T. Postek, final report to International SEMATECH, January 2003, available to member companies at SEMATECH Web site.

3. "Dimensional Metrology of Resist Lines using a SEM Model-Based Library Approach," J. S. Villarrubia, A. E. Vladár, B. D. Bunday, and M. Bishop, Submitted to Proc. SPIE **5375**, 199-209 (2004).

4. J. S. Villarrubia and B. D. Bunday, "Unbiased Estimation of Linewidth Roughness," *Proc. SPIE* **5752** (2005), in press.

5. "Scanning electron microscope dimensional metrology using a model-based library," J. S. Villarrubia, A. E. Vladár, and M. T. Postek, Surface and Interface Analysis, in press.

6. "Influence of Focus Variation on Linewidth Measurements," M. Tanaka, J. S. Villarrubia, and A. E. Vladár, *Proc. SPIE* **5752** (2005), in press.

7. "Tip Characterization for Dimensional Nanometrology," J. S. Villarrubia, in *Applied Scanning Probe Methods,* eds. B. Bhushan, H. Fuchs, and S. Hosaka (Springer-Verlag, Berlin Heidelberg 2004) p. 147.

8. "A Simulation Study of Repeatability and Bias in the CD-SEM," J. S. Villarrubia, A. E. Vladár, and M. T. Postek, submitted to Journal of Microlithography Microfabrication, and Microsystems. (This is an updated reprint of the "Metrology Best Paper" at the 2003 SPIE Microlithography Symposium.)

9. "Issues in Line Edge and Linewidth Roughness Metrology," J. S. Villarrubia, submitted for proceedings of the 2005 International Conference on Characterization and Metrology for ULSI Technology, Richardson, TX March 15-18, 2005.

# Atom-Based Dimensional Metrology

**Technical Contact:**
R. Silver

## Goals

Provide technological leadership to semiconductor and equipment manufacturers and other government agencies by developing the methods, tools, and artifacts needed to apply leading edge, high-resolution atom-based dimensional measurement methods to meet the metrology needs of semiconductor microlithography. One specific goal is to provide the customer with the techniques and standards needed to make traceable dimensional measurements on wafers with nanometer accuracy. We are developing nanometer-scale three-dimensional structures of controlled geometry whose dimensions can be measured and traced directly to the intrinsic crystal lattice. These samples are intended to be dimensionally stable to allow transfer to other measurement tools which can measure the artifacts with dimensions known on the nanometer scale.

## Customer Needs

This project responds to the U.S. industry need for length intensive measurement capabilities and calibration standards in the nanometer scale regime. The new class of scanned probes have unparalleled resolution and offer tremendous promise for meeting these future measurement, test artifact, and calibration standards needs of the microelectronics industry. One important application of the high-resolution SPM methods is in the development of test artifacts and linewidth standards whose dimensions can be measured and traced through the crystal lattice from which they are made. In addition, these high-resolution tools can be coupled directly to a new NIST-designed picometer resolution interferometer (Fig. 1).

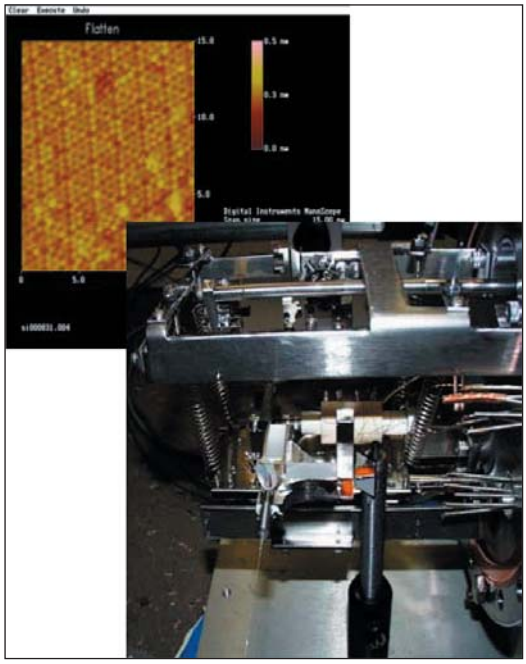


*Figure 1. The atomic resolution image above was measured with a 20 pm resolution interferometer system mounted on the UHV STM.*

The work funded in this project is for the development of atom-based test artifacts and linewidth standards to assist in the development of high-resolution imaging techniques and calibration of linewidth metrology tools. We are also developing unique high-resolution interferometry capabilities which can be used in conjunction with accurately measured tips to measure feature critical dimensions at the nanometer scale. One focus of the research is to enable the accurate counting of atom spacings across a feature in a controlled environment and to subsequently transfer that artifact to other measuring instruments as a structure with atomically known dimensions.

An essential element of this project is the fabrication of test artifacts and structures for the development of high resolution imaging methods. It is imperative to enable fabrication methods for sub-10 nm sized features. Several recent developments in optical microscopy, scatterometry and SEM metrology require test samples with critical dimensions below 10 nm. These test structures are simply not available at this time. In this project we are developing the methods for fabrication of sub-10 nm sized features and etching methods to transfer these patterns into the silicon substrates (Fig. 2).

As critical dimensions continue to shrink, the detailed atomic structure, such as edge roughness or sidewall undercut, of the features to be measured represents a larger portion of the measurement uncertainty. Furthermore, particularly with SEMs and optical CD tools, the instrument response and the uncertainty in the edge location within an intensity pattern becomes a significant issue due to the increased sensitivity to detailed elements of the edge detection model. The complexity of these physics-based scattering models and large computer resources required for each individual computation make the concept of having samples of known geometry and width essential. This project is developing samples of

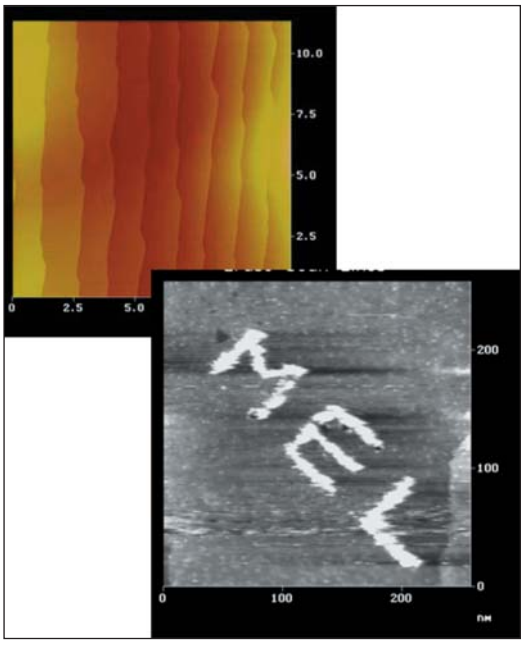


*Figure 2. This recent result utilizes the atomically flat surfaces as a substrate for nanomanufacturing. The featured CDs are 10 nm and the entire lateral field of view is 250 nm. The background shows an atomically flat substrate.*

known geometry and atomic surface structure which yield well defined dimensional measurements. One goal is a measurement which results in a specific number of atoms across the line feature or between features. The process being developed allows for samples to be measured in the UHV environment and then stabilized and subsequently transferred to other instruments (Fig. 3).

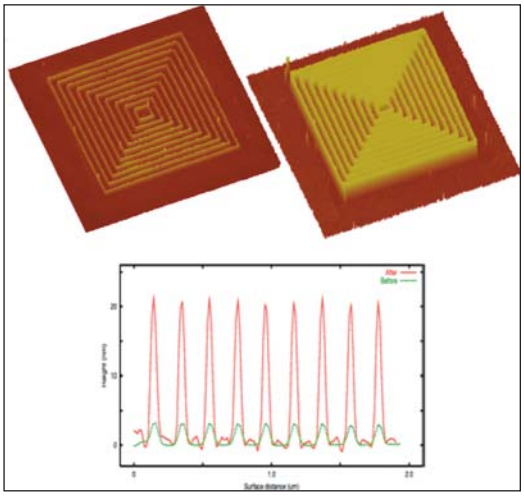

*Figure 3. A demonstration of the nanofabrication process with an RIE process used to transfer the patterns into the silicon substrate.*

These methods of atom counting and high-resolution interferometry, as outlined in this project description, are non-destructive and are intended to yield samples which can be measured by various instruments such as an SEM optical CD tool with subsequent re-measurement on the atomic scale. This is a unique and important element of this work since there are no other known methods that allow this kind of atomic dimensional measurement without being destructive. In addition, this new method opens up the possibilities of basing the measurement metric on the intrinsic crystal lattice.

## Technical Strategy

The technical work is focused into four thrust areas.

1. The development of methods to prepare photolithographically patterned three-dimensional structures in semiconductor materials. These structures are being prepared in silicon to allow the atomic surface order which is commensurate with the underlying crystal lattice. This involves either using conventional photolithography methods for sample production or using the STM itself to fabricate very small nanometer scale features as shown in Fig. 2.

**DELIVERABLES:** Write features in silicon with critical dimensions smaller than 10 nm. Apply the pattern writing process and etch features for use as optical scatterfield test structures. 3Q 2005.

**DELIVERABLES:** Work with EEEL to develop improved methods for etching nanostructures written in silicon. Use RIE etching techniques to etch features with sub-10 nm dimensions in silicon. 3Q 2005.

2. The development of techniques for the preparation of SPM tips with reproducible geometries and the direct characterization of the SPM tip geometry and dimensions on the atomic scale. These well characterized tip probes can then be used to measure the samples with photolithographically defined and canonically ordered surfaces on the sub-nanometer length scale. We are developing the SPM tip etching, field evaporation, and cleaning procedures which reliably yield stable W tips and produce atomic resolution on Si (7x7) surfaces. These tips are also useful in a collaboration with the SEM project for development as nanotips as SEM field emitters. Our tip preparation methods leave us uniquely qualified in this arena.

**DELIVERABLES:** Investigate nanotubes and alternative W tips as for use in high resolution imaging. Determine the stability of nanotubes for use as STM imaging and fabrication tips. 1Q 2005.

3. Focus on the development of artifacts that can be atom counted and then measured in a number of different metrology tools such as SEM and AFM. The integrity of the line geometry, such as side wall angle, is crucial to having useful artifacts for linewidth specimens. These edge geometry requirements are not as stringent for the magnification standards since feature symmetry is the most crucial element in these measurements. The work on linewidth artifacts, therefore, is focused on reducing the process temperatures required for atomic reconstructions. We have made wet chemical processing fully operational and have also demonstrated atomically ordered Si surfaces at significantly reduced temperatures. For sample preparation, we are utilizing the existing *in-situ* processing apparatus and techniques from the UHV STM and concentrating on the reproducible production of atomically ordered Si surfaces and Si (111) step and terrace structures (Fig. 4).

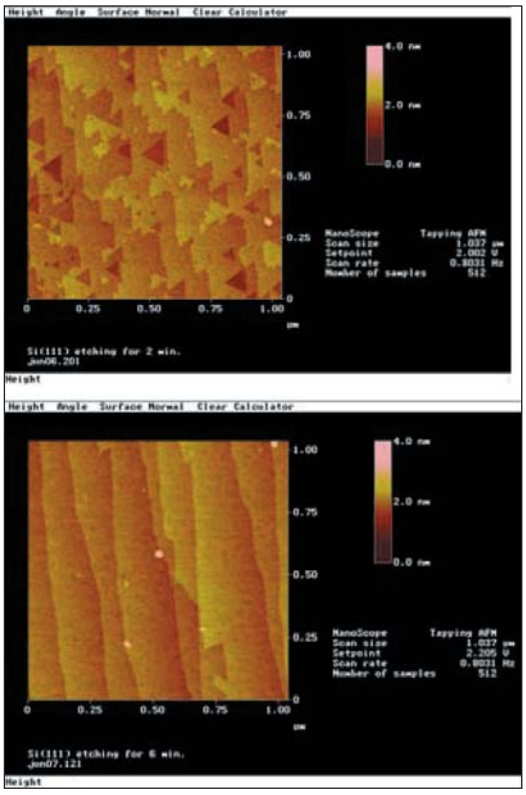


*Figure 4. These are atomically flat, chemically prepared surfaces for use in atom-counting and nanomanufacturing.*

**DELIVERABLES:** A new STM which has improved atomic scale imaging capability for atom-based dimensional metrology has been procured and delivered. Implement a transfer mechanism for sample transfer into the UHV environment with the new STM to enable fabrication and metrology on the atomic scale. Install the new STM into the UHV system, test and characterize the new STM and make fully operational. 2Q 2005.

4. The development of a new interferometer system capable of measuring dimensions in the 20 picometer range with high accuracy. Develop an improved system which is also capable of use on the STM so atomic scale measurements can be made with new levels of accuracy. Explore new applications of field ion microscope (FIM) calibrated tips in conjunction with the interferometry to measure CDs of leading edge, small semiconductor features.

The long term technical objective is the development of *in situ* stabilized, atomically ordered surfaces that can be transferred to other measurement instruments such as scanning electron microscopes, AFMs, or optical metrology tools. These nanometer-scale standard artifacts with atomically ordered surfaces will then act as linewidth or magnification calibration samples. These samples will have been measured either by direct atom counting or high-resolution interferometry and atomically measured tips.

## Accomplishments

- We have prepared atomically flat surfaces and obtained atomic order on the wet chemical prepared surfaces. The routine imaging of these surfaces on the atomic scale should be enhanced with the new STM currently being implemented.

- The ability to prepare atomically sharp tips in W (111) has been demonstrated. The details of this methodology and the new models we have developed for analyzing sharpness have been published as an archived journal article.

- Develop the advanced modeling requirements to fully simulate the new STM structure. We have completed finite element analysis (FEA) simulations which test the dynamic modes of the STM and interferometer structure. These results have significantly improved the structural designs.

The results, seen in figure 4, yield a new, more comprehensive understanding of the physical processes involved in making atomically flat surfaces in silicon as required for much of the work in this project.

■ The etching process has been developed and demonstrated for patterns written on silicon. Patterns with features as small as 10 nm have been written in hydrogen terminated silicon surfaces with subsequent pattern transfer into the silicon substrates. A publication recently appeared on this material.

■ We have used the FIM techniques to analyze nanotubes and their structure. The nanotubes were directly characterized for use as SPM tips with dimensional analysis on the atomic scale. We are now applying these ideas to FIM tips used in SEM metrology (Fig. 5).

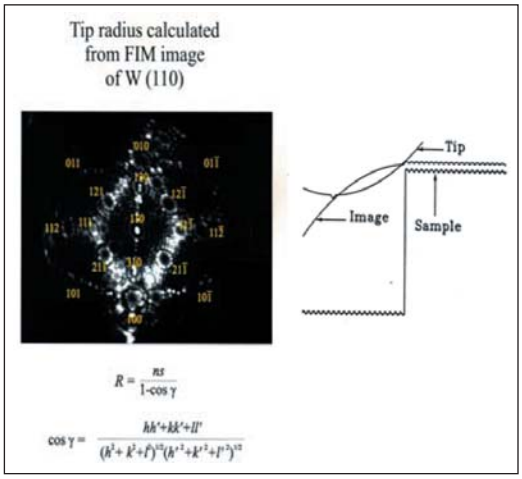


*Figure 5. An FIM image showing the atomic order in a W tip is shown. The schematic on the right shows the method of atom counting or high resolution tip-based interferometry.*

■ We have measured directly the surface atom spacings based on an interferometer measurement. We have fitted our UHV STM with a high accuracy sub angstrom resolution interferometer. We have closed the loop and made atomic resolution measurements with full interferometer length basis. The successful completion of this aspect has enabled direct distance determination with simple atomic counting.

**ACCOMPLISHMENT:** The results for the first demonstration of direct interferometer measurements of surface atom spacings with a complete unbroken uncertainty have been published in Optical Engineering. These results were also presented at the ASPE conference and SPIE to make the new interferometry methods available to the industry.

## Collaborations

ISMT, IBM, University of Maryland, Dept. of Physics, University of Purdue, Dept. of Physics., George Washington University.

## Recent Publications


H. Zhou J. Fu, and R. M. Silver "The Influence of Defects on the Morphology of Si (111) Etched in $NH_4F$," to be submitted, Journal of Chemical Physics (2005).

J. Gilsinn, H. Zhou, B. Damazo, J. Fu, R. Silver, Nano-Lithography in Ultra-High Vacuum (UHV) for Real World Applications, Proc. Nanotech 2004.

J.A. Dagata, C.A. Richter, R.M. Silver, E. Vogel, J.V. Martinez de Pinillos, "Metrology Development for the Nanoelectronics Industry at the National Institute of Standards and Technology," Proc. NanoTech 2004.

H. Zhou, "Study of wet chemically prepared hydrogen terminated Si (111) surfaces and a novel implementation of a high resolution interferometer," Thesis, University of Maryland, 2004.

R. M. Silver, S. Gonda, J. Jun, L. Howard, and C. Jensen, "Atomic Resolution Measurements with a New Tunable Diode Laser-Based Interferometer," Optical Engineering, Vol. 43 No. 1 (Jan. 2004).

P. V. M. Rao, C. P. Jensen, and R. M. Silver "An enhanced model for STM tip geometry measured with FIM," JVST B (Mar/Apr 2004).

Brad Damazo, Hui Zhou, Satoshi Gonda, and Richard M. Silver, "New Tunable Diode Laser-based Interferometer," ASPE Conf. Proc. 2003.

J. Fu, H. Zhou, J. Kramar, S. Gonda and R. M. Silver "Dependence of Morphology on Miscut Angle for Si(111) Etched in NH4F," Applied Physics Letters, Vol. 82, No. 18 (2003).

"Nanomanufacturing of Atom Based Standards," NAMT final report. NISTIR 6850 (2002).

J. Gilsinn, B. Damazo, R. Silver, and H. Zhou "A Macro-micro Motion System for a Scanning Tunneling Microscope," World Automation Congress, Proc. From Int'l. Symp. on Robotics and Applications (2002).

Satoshi Gonda, Hui Zhou, Joseph Fu and Richard M. Silver, "A new design and uncertainty consideration of a metrology UHV-STM for direct measurements of atom spacings," Proc. SPIE Nanotechnology workshop Vol. 4608 p. 125 (2002).

Hui Zhou, Joseph Fu, S. Gonda and Richard M. Silver "Effects of Etching Time and Wafer Miscut on the Morphology of Etched Si(111) Surfaces," Proc. SPIE Nanotechnology workshop Vol. 4608 p. 168 (2002).

# Wafer-Level and Overlay Metrology

**Technical Contacts:**
R. Silver
T. Doiron

## Goals

Provide technological leadership to semiconductor in equipment manufacturers, and other government agencies by developing and evaluating the methods, tools, and artifacts needed to apply optical techniques to the metrology needs of semiconductor microlithography. One specific goal is to provide the customer with the techniques and standards needed to make traceable dimensional measurements on wafers at the customer's facility. The industry focus areas of this project are primarily the optical based methods used in overlay metrology and optical, wafer level critical-dimension (CD) metrology.

## Customer Needs

Tighter tolerances on CD measurements in wafer production place increasing demands on linewidth accuracy and on overlay tolerances. A recent industry focus on high throughput, lower cost of ownership metrology tools, which enable more dense sampling strategies has lead to a comprehensive program at NIST to both support and advance the optical techniques needed to make these overlay and photomask/wafer critical dimension measurements (see Fig. 1).

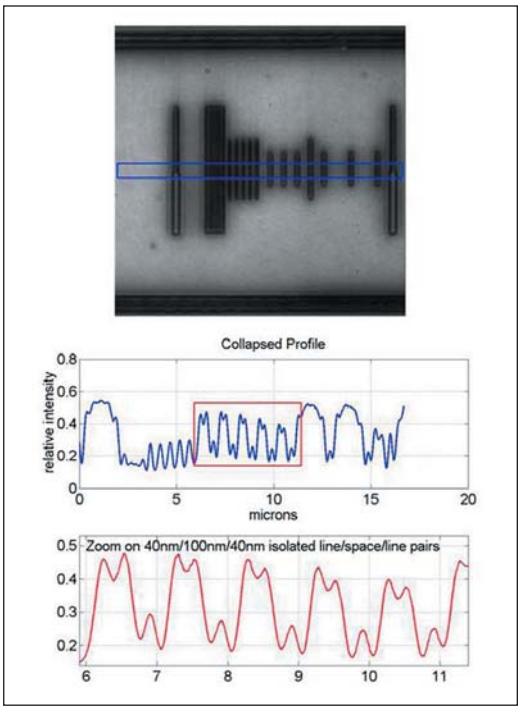


*Figure 1. An optical image and profiles of sub-40 nm CD targets used in the development of new advanced high-resolution optical techniques.*

*Improved two-dimensional overlay measurement techniques and standards are needed for measuring and controlling overlay capabilities of steppers and separating out the contributions from the photomask. Overlay is listed in Table 115 of the 2004 Update SIA ITRS as a difficult challenge for both >45 nm and <45 nm processes. Overlay improvements have not kept pace with resolution improvements and will be inadequate for ground rules less than 65 nm. In fact, Table 117b shows that no known solutions for overlay output metrology exist beyond the 65 nm node. As shown in Table 118a, the problems are more acute for CD metrology where the industry is currently encountering metrology problems without known manufacturing solutions.*

## Technical Strategy

There are two main strategic technical components of this project.

1. NIST has developed an overlay metrology tool that has undergone continuous development of the mechanical hardware, optical components, and measurement algorithms to obtain uncertainties comparable to or better than the best industry overlay tools. This optical metrology tool is now used to calibrate standards and to support the development of improved measurement algorithms and alignment techniques. The technical strategy for overlay metrology is divided into two segments: (a) instrumentation development and the advance of overlay metrology techniques, and (b) the design and calibration of standard artifacts. Pattern placement and overlay of the various lithographic levels is monitored with a series of targets, each in a different plane. The overlay offset is then obtained by optical measurements with a determination of the relative target centerlines. Any misalignment in the overlay metrology system will translate into an artificial overlay offset, referred to as *tool induced shift* (TIS). Additionally, there are residual errors caused by asymmetries in the target edges or covering layers (resist) known as *wafer induced shift* (WIS) (Fig. 2, pg. 58).

A set of standard artifacts and procedures, development at NIST, has been implemented to assist in aligning overlay measurement systems and minimizing TIS. After alignment, the tool must then be calibrated with standard artifacts to yield accurate overlay offsets. The measurement

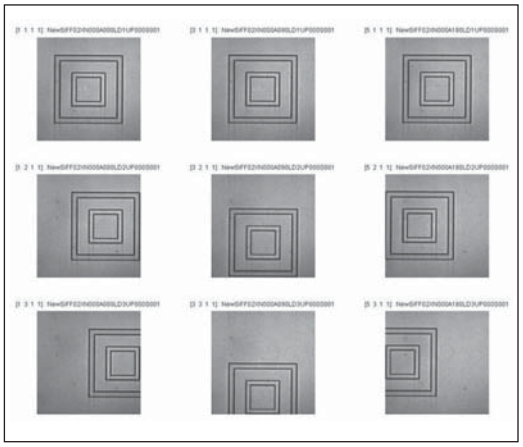

*Figure 2. An example of reversal methods applied to determine WIS and the asymmetry of the target itself.*

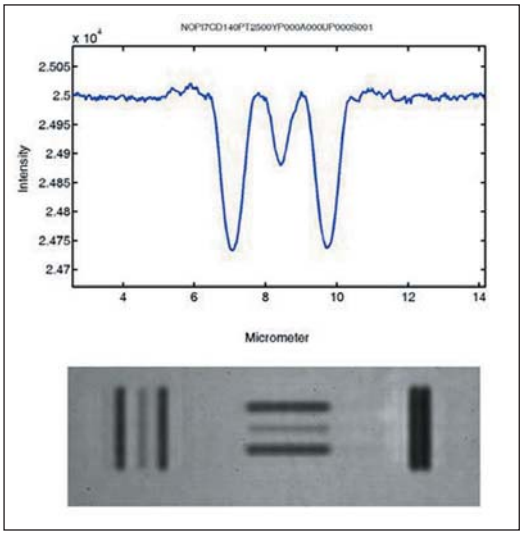


*Figure 3. The new in-chip overlay targets.*

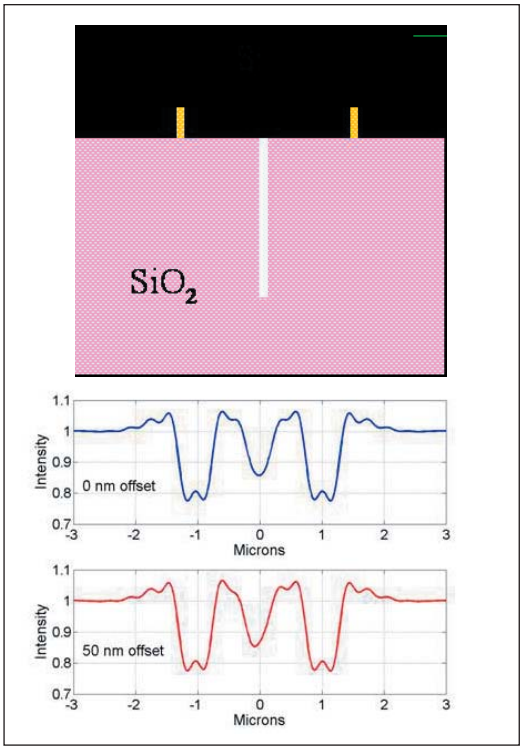


*Figure 4. New proposed overlay targets which occupy less than 2 μm x 2 μm in total space. This is designed to be an in chip target.*

system used for this component is an optical reflection mode instrument, typically operated in a bright field mode. The hardware includes high resolution image capture with a full field CCD data acquisition system which has been fully characterized and calibrated. This instrument has enabled a detailed study of CCD array performance and characterization. In this work, several CCD acquisition systems have been evaluated and improved edge detection and CCD array calibration procedures have been implemented. These same methods for two-dimensional CCD array analysis are now being applied to optical component alignment error and aberration analysis.

WIS-free standard overlay artifacts have been fabricated in 200 mm and 300 mm wafers. These overlay artifacts are for the calibration of industrial optical overlay tools. The artifacts have been fabricated in single crystal silicon and provide an array of etched silicon three-dimensional targets. These wafers additionally have an extensive set of characterization targets and research structures developed in close collaboration with SEMATECH and leading semiconductor manufacturers, for example, Fig. 3 and Fig. 4.

We are also developing a new set of in-chip overlay targets intended to enable the measurement of overlay throughout the active area of a die. These results have been published recently and collaborative work is progressing to develop the commercial capabilities to measure overlay using device sized features in targets of small overall dimension. There is also a comprehensive effort to develop new high resolution overlay targets intended to enable the continued use of optical overlay measurements for the 65 nm node and beyond.

**DELIVERABLES:** Complete an improved set of qualification tests for the overlay microscope, optics, and the *x-y* metrology stage. Submit the final uncertainties and tabulated combined uncertainty values to the SRM office in an SP260. This includes the characterization and calibration of complex optical alignment effects on overlay output values. 2Q 2005

**DELIVERABLES:** Use the new metrology reticles from the SEMATECH collaboration to fabricate a new set of overlay calibration targets/wafers. Work with SEMATECH and the Overlay Metrology Advisory Group (OMAG) to determine designs of new high resolution overlay targets. This includes design elements and measurement protocols for using the new high resolution overlay targets to enable optical metrology beyond the 65 nm node. 4Q 2005

**DELIVERABLES:** Work with SEMI and SEMATECH in the development of new target designs and standards specifications for overlay metrology. This new specification will try to bring some standardization to the growing number of proprietary overlay target designs. 4Q 2005

Modeling the effects of all of the relevant feature properties encountered in overlay measurements and optical critical dimension measurements using existing and new software tools, can yield significant improvements in measurement accuracy, as in Fig. 5. NIST has a world class effort in optical modeling. This includes the comprehensive comparison of two rigorous coupled wave guide scattering models, a finite difference time domain-based model and the NIST-developed exact integral equation solver method. The latter method has become recognized as the most accurate in existence today.

**DELIVERABLES:** Compare and test the accuracy of new scattering models for line width evaluation in reflection mode and transmission mode. 3Q 2005

**DELIVERABLES:** Develop new calculation methods for analyzing asymmetric overlay targets. Compare with modeling results of more standard double-etched silicon structures. 2Q 2005

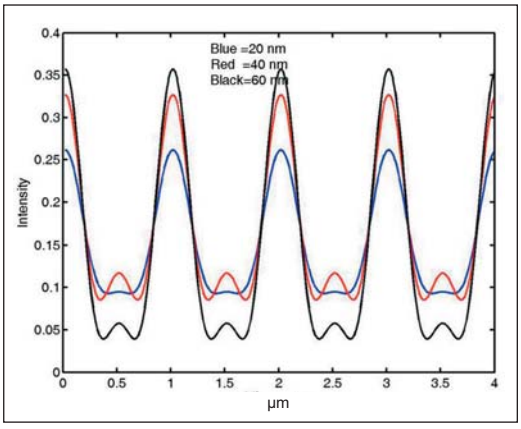


*Figure 5. These data are modeling results showing the potential for using high resolution optical methods for wafer level CD metrology.*

2. The second component of this project is the development of new, advanced high-resolution optical metrology techniques. A new class of optical measurement techniques known as scatterfield microscopy is being developed at NIST. This methodology has demonstrated the possibility of using optical methods for line width and overlay metrology with targets smaller than 50 nm critical dimensions. This new approach utilizes structured illumination in parallel with engineered target designs. The technique is well suited to the use of specific metrology targets as encountered in semiconductor manufacturing.

A key element of this approach is to develop optical methods which can be suitably applied to device sized features. Current metrology requirements are demanding higher throughput, non-destructive measurements with nanometer sensitivity to enable tighter process control as well as closed-loop integrated process control. The current class of scatterometry and scatterfield optical techniques are promising, potential solutions to these significant metrology challenges. As a part of this project, we are developing a new optical tool specifically intended to enable this type of scatterfield measurement. This includes comprehensive modeling as well as a new optical configuration designed in house. The optical design work includes a thorough examination of illumination effects and accurate methods to prepare optical illumination fields.

**DELIVERABLES:** Develop a comprehensive set of techniques to accurately measure optical illumination fields. Develop similar characterization methods to measure the collection optics set of aberrations and to perform optimum optical alignment. 3Q 2005

**DELIVERABLES:** Develop fully automated focus and positioning control systems for the new scatterfield microscope. Complete the optical component design and layout for the new tool and assemble the illumination optics in an open architecture configuration. Implement the existing comprehensive analysis capabilities for data acquisition and edge detection methods. 4Q 2005

## Accomplishments

■ **Researchers from the overlay metrology project have submitted two CD 240s** for the disclosure of recent potential breakthrough material in high resolution optical metrology. As a part of this disclosure, a new target design which occupies only a few square microns of space was unveiled. The second CD 240 focused on a new proposed method for CD metrology using through-focus

focus-metric signatures which have shown near to nm scale sensitivity to changes in linewidth.

■ **NIST electromagnetic scattering code:** In a further development of the very successful application of the NIST electromagnetic scattering code developed by E. Marx, new results involving arrayed targets have been obtained. These model extensions are providing simulations results and guidance in the optical metrology of targets with features currently down to 70 nm. The model is now capable of simulating targets in array formats as well as illumination at a single angle for analysis and development of scatterfield methods.

■ **Competence proposal successfully funded:** The optics project was successful as champion for the Scatterfield competence proposal. A significant effort to put together and optimize the cross laboratory proposal was successful in landing long term funding for the Scatterfield work. Several companies have shown interest in this work. The funding involves collaboration between the Manufacturing Engineering (MEL) and Physics (PL) laboratories for the evaluation and development of high resolution optical methods involving scatterometry and the new scatterfield methods being developed within Precision Engineering Division (PED). The work also involves technical evaluation of the key issues associated with optical modeling and the n and k input parameters.

■ **Significant industry interest in new high-resolution optical methods being developed under the Scatterfield Microscopy title.** Following invited presentations at SEMATECH OMAG and Advanced Metrology Advisory Group (AMAG) metrology workshops, and discussions at SPIE, there was much interest in the surprising results of 40 nm sized features. These results obtained by optical methods are some of the smallest features shown to these audiences and go well beyond the expected capabilities of these tools.

■ **Reflection mode optical measurements of phase shifting photomasks**. The first round of measurements and model comparisons between profiles from phase shifting reticles has been completed. These results obtained in reflection mode have compared experimental measurements with modeling results obtained using the Egon Marx electromagnetic scattering code. These results were documented and summarized in a SEMATECH final report.

■ **The NIST Overlay Metrology project leader has played a significant role in the (OMAG) of SEMATECH**. This group is developing a comprehensive set of measurement guidelines, test methods, and tool performance measures to be adopted by the semiconductor manufacturing industry. The group is made up of more than 15 international semiconductor manufacturers and tool suppliers. The OMAG has strong interest in adopting several new methods developed in the NIST Overlay Metrology Project. In particular, the recently published methods for evaluating in-chip and devise sized overlay targets. In addition, CCD array performance and overall optical system characterization and calibration performance measures developed at NIST have been adopted.

■ **Members of the optical metrology project met with several leading optical metrology tool manufacturers** and international measurement laboratories regarding recent advances in the scatterfield microscopy technique. The individual discussions included details about the new high resolution microscopy techniques being developed at NIST and their potential industrial application and implementation. Research in the area of high resolution optical methods is now being pursued at several companies with clear applications in overlay metrology and potential applications in optical based critical dimension metrology. The discussions largely focused on potential technology transfer between the NIST optical projects and development scientists at the optical metrology companies. Details on recent techniques for optical aberration measurements and on methods for evaluating Kohler illumination were covered

■ **NIST researchers have made model comparisons** between the E. Marx developed optical scattering code with the Spectel company Metrologia metrology modeling package and the new modeling package from Rsoft. Different material systems were compared as well as one overlay feature at different focus positions. New results, based on the full integration of the NIST scattering code and Spectel optical microscope model, show very good agreement. This is an important step in the effort to provide industry the quantitative ability to determine sample-dependent effects on overlay tool performance. Results have been presented at SPIE Microlithography.

■ **The clean room enclosure for the overlay metrology tool is fully operational.** The metrology tool has been moved to the Advanced Metrology Laboratories and has been returned to its fully operational state in the improved vibration and

cleanliness environment. This allows us to work closely with the industry and make SRMs directly transferable to a clean room environment.

## Collaborations

ISMT, IBM, IVS Schlumberger, KLA-Tencor, Intel, Motorola, AMD and several other leading manufacturers or tool vendors.

The 14 members of The Neolithography Consortium.

## Recent Publications


R. M. Silver, R. Attota, M. Stocker, M. Bishop, L. Howard, M. Davidson, T. Germer, and R. Larrabee, "High-resolution Optical Metrology," SPIE Vol. 5752, (2005).

R. Attota, R. M. Silver, T. Germer, M. Bishop, R. Larrabee, M. Stocker, L. Howard, "Application of Through-focus Focus metric Analysis in High-resolution Optical Metrology," SPIE Vol. 5752 (2005).

R. M. Silver, R. Attota, M. Stocker, M. Bishop, J. Jun, E. Marx, M. Davidson, and R. Larrabee, "High-resolution Optical Overlay Metrology," SPIE Vol. 5375 P. 78 (2004).

R. Attota, R. M. Silver, M. Bishop, E. Marx, J. Jun, M. Stocker, M. Davidson, R. Larrabee, "Evaluation of new in-chip and arrayed line overlay target designs," SPIE Vol. 5375 P. 395 (2004).

J. M. Pedulla, J. Potzick, R. Silver, and R. Larrabee, "Improving the Uncertainty of Photomask Linewidth Measurements," SPIE Vol. 5375 P. 317 (2004).

R. Attota, R. Silver, M. Stocker, M. Bishop, J. Jun, E. Marx, and M. Davidson, "A New Method to Enhance Overlay Tool Performance," SPIE Vol. 5038 P. 428 (2003).

R. Silver, M. Stocker, R. Attota, J. Jun, E. Marx, R. Larrabee, and M. Davidson, "Calibration Strategies for Overlay and Registration Metrology," SPIE Vol. 5038 P. 103 (2003).

R. Silver, R. Attota, M. Stocker, J. Jun, E. Marx, R. Larrabee, B. Russo, and M. Davidson, "Comparison of Measured Optical Image Profiles of Silicon Lines with Two Different Theoretical Models," SPIE Vol. 4689 (2002).

B. Russo, M. Bishop, D. Benoit, and R. Silver, "Overlay Tool Comparison for sub-130nm Technologies," SPIE Vol. 4689 p. 261 (2002).

"Overlay Benchmarking Report," ISMT 2002, B. Russo, R. Silver *et al*.

J. Seligson, B. Golovanevesky, J. Popawski, M. Adel, and R. Silver, "Overlay Metrology simulations – Analytical and experimental validations," Proc. SPIE Vol. 5038 P. 61 (2003).



R. Silver, M. Stocker, R. Attota, J. Jun, E. Marx, R. Larrabee, and M. Davidson, "Calibration Strategies for Overlay and Registration Metrology," SPIE Vol. 5038 P. 103 (2003).

R. Attota, R. Silver, M. Stocker, M. Bishop, J. Jun, E. Marx, and M. Davidson, "A New Method to Enhance Overlay Tool Performance," SPIE Vol. 5038 P. 428 (2003).